

MODEL NAME : ZAP00  
PROJECT CODE : ANRZAP0000  
PCB NO : DA8000WL000 LA-A301P M/B  
DA4001XN000 LS-A301P LOGO/B  
DA4001XO000 LS-A302P IND/B  
DA4001XP000 LS-A303P BTN/B  
DA4001XQ000 LS-A304P NGFF/B  
FPC NO : LF-A301P HEAD/B  
LF-A302P SLIT\_R/B  
LF-A303P SLIT\_L/B  
LF-A304P KB/B

# Compal Confidential Schematic Document

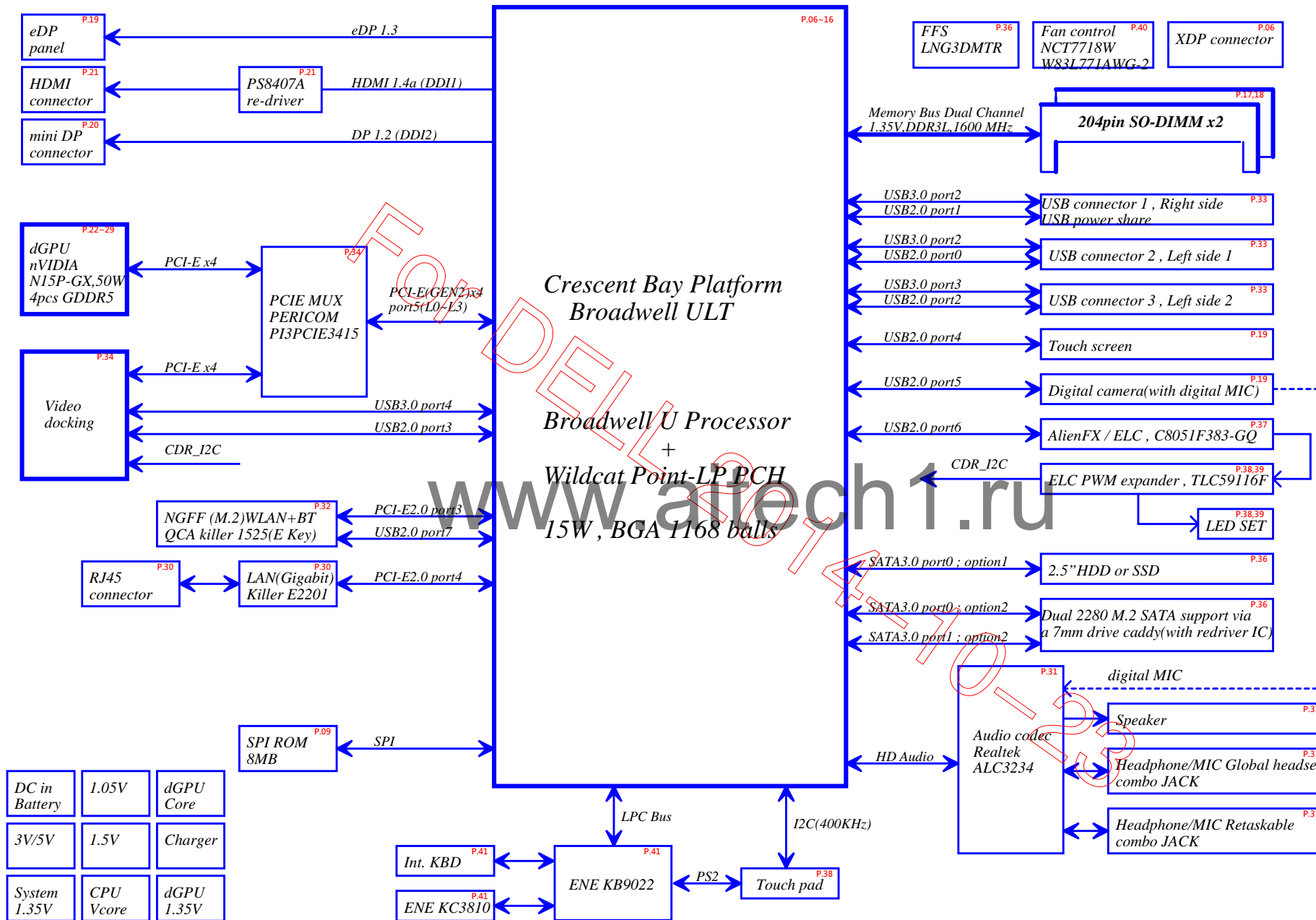
Crescent Bay Platform  
Intel Broadwell ULT  
2014-09-23

Rev: 1.0

X76@ : 76 level  
46@ : 46 level  
@ : Nopop component  
CONN@ : Connector component  
XDP@ : XDP function  
EMI@ : EMI parts  
@EMI@ : Reserve EMI parts  
ESD@ : ESD parts  
@ESD@ : Reserve ESD parts  
RF@ : RF parts  
BDWI5@ : CPU BDW I5  
H@:Haswell  
B@:Broadwell



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		LA-A301P		Date	Thursday, September 25, 2014
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Board ID Table for AD channel

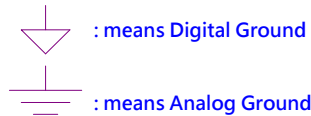
Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

NVIDIA  
GraphicAMD  
Graphic

Board ID table and PCB version

ID	Rb	HSW(Haswell)	BDW(Broadwell)
0	0	EVT-1(R0.1) , EVT-2(R0.1)	EVT-1(R0.1)
1	12K	EVT-3(R0.2)	EVT-2(R0.2)
2	15K	DVT-1(R0.3) , DVT1.1(R0.4)	DVT-1(R0.5)
3	20K	DVT-2(R0.5)	Not use
4	27K	Not use	DVT-1.1(N16P,R0.6)
5	33K	Not use	DVT-2(R1.0)
6	43K	Pilot(R1.0)	Pilot(R1.0)

Symbol Note :



CLOCK SIGNAL

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	M.2 Card WLAN
CLKOUT_PCIE3	10/100/1000 LAN
CLKOUT_PCIE4	N15P-GX , Video docking
CLKOUT_PCIE5	

USB3.0

Port1	Left side 1
Port2	Right side (power share)
Port3	Left side 2
Port4	Caldera

USB2.0

Port0	Left side 1
Port1	Right side (power share)
Port2	Left side 2
Port3	Caldera
Port4	Touch screen
Port5	Camera
Port6	ELC
Port7	BT

PCI EXPRESS

Lane 1	
Lane 2	
Lane 3	WLAN(M.2 Card)
Lane 4	10/100/1000 LAN
Lane 5	PCIE 4x MUX
Lane 6	

SATA

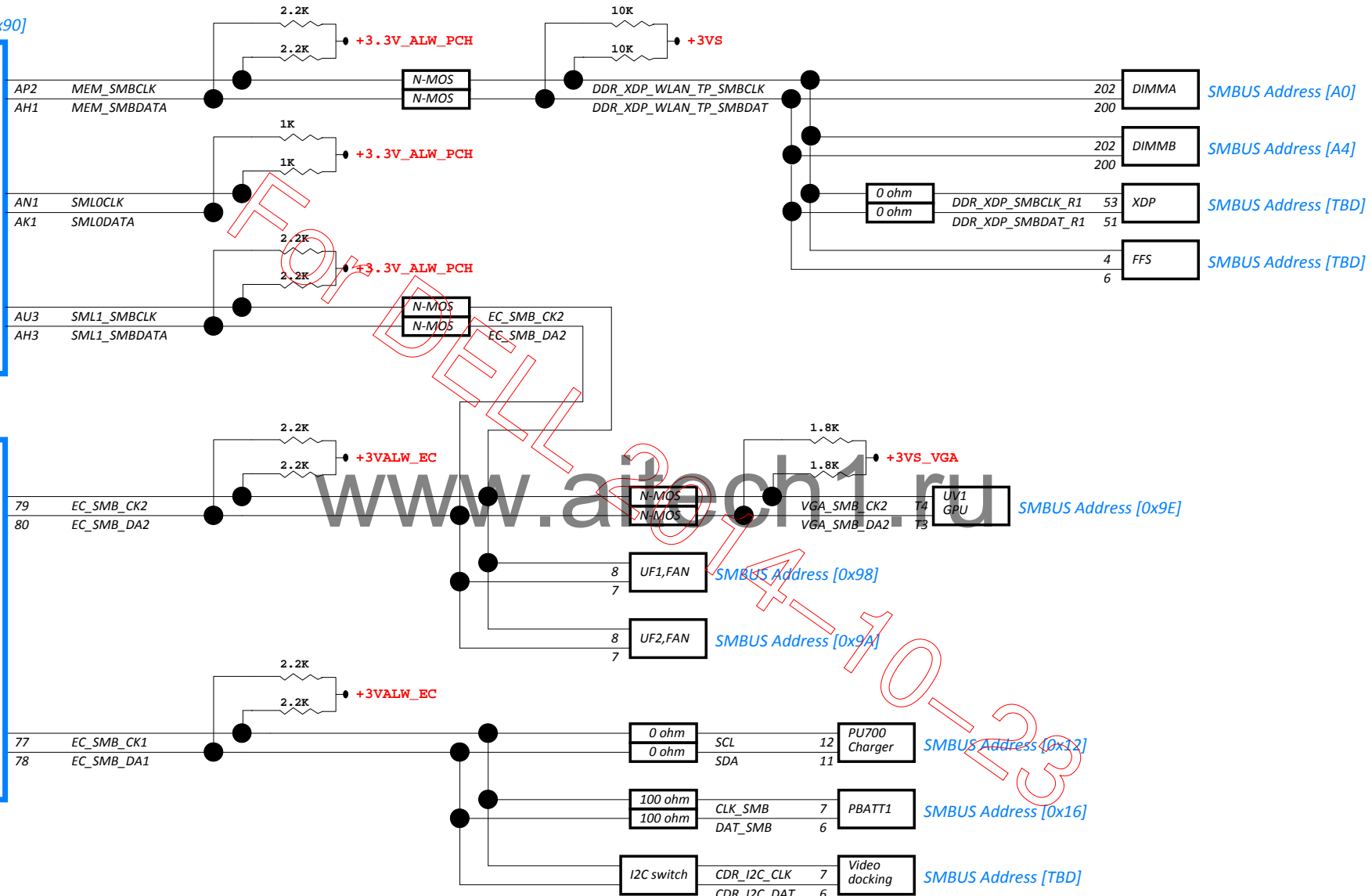
SATA0	HDD or NGFF SSD1
SATA1	NGFF SSD2
SATA2	
SATA3	

ULT

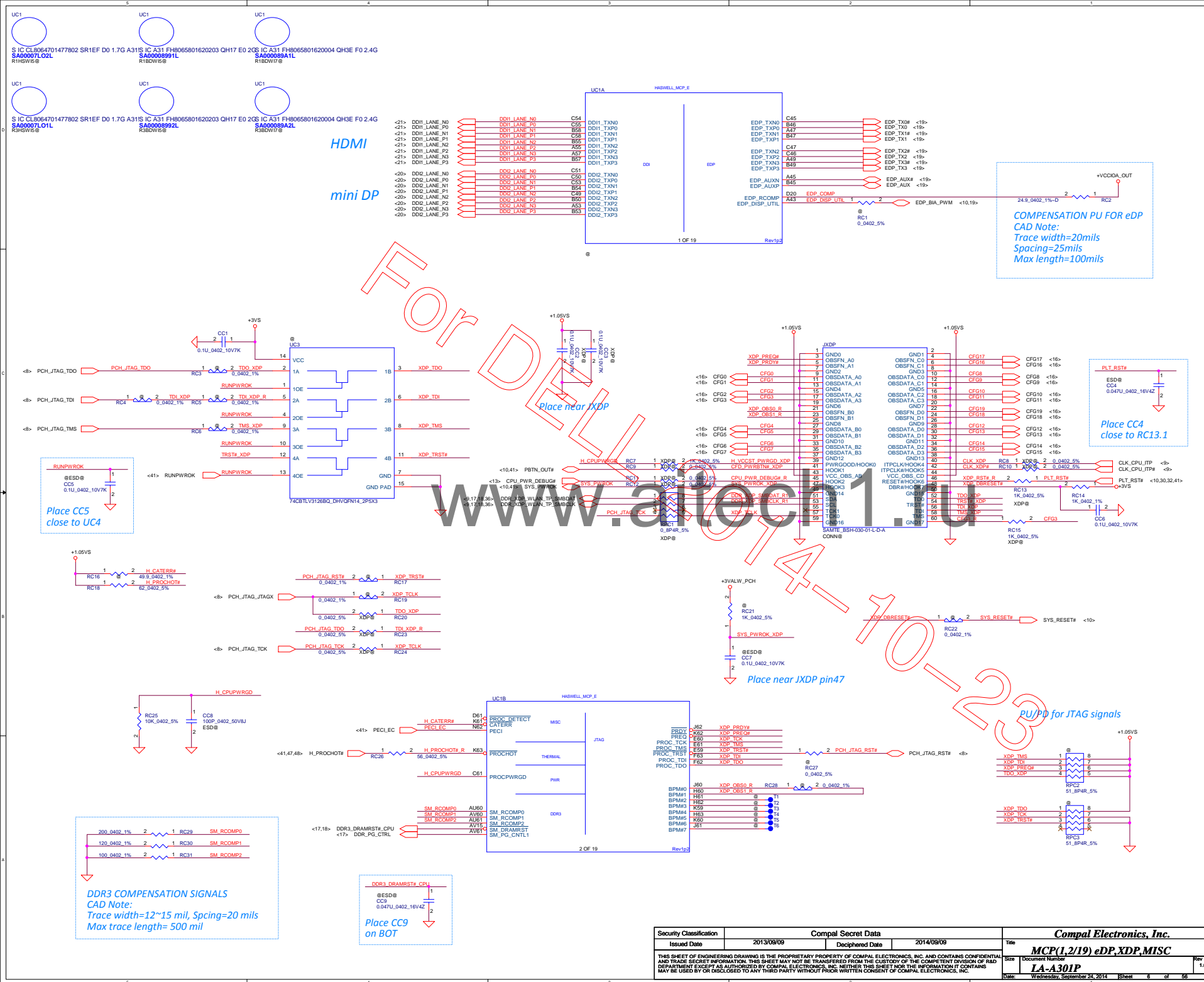
SMBUS Address [0x90]

ULT  
Broadwell

KBC  
KB9012A4

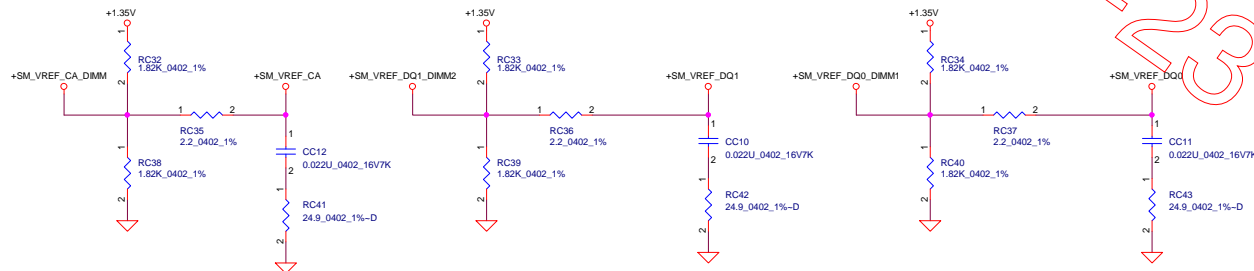
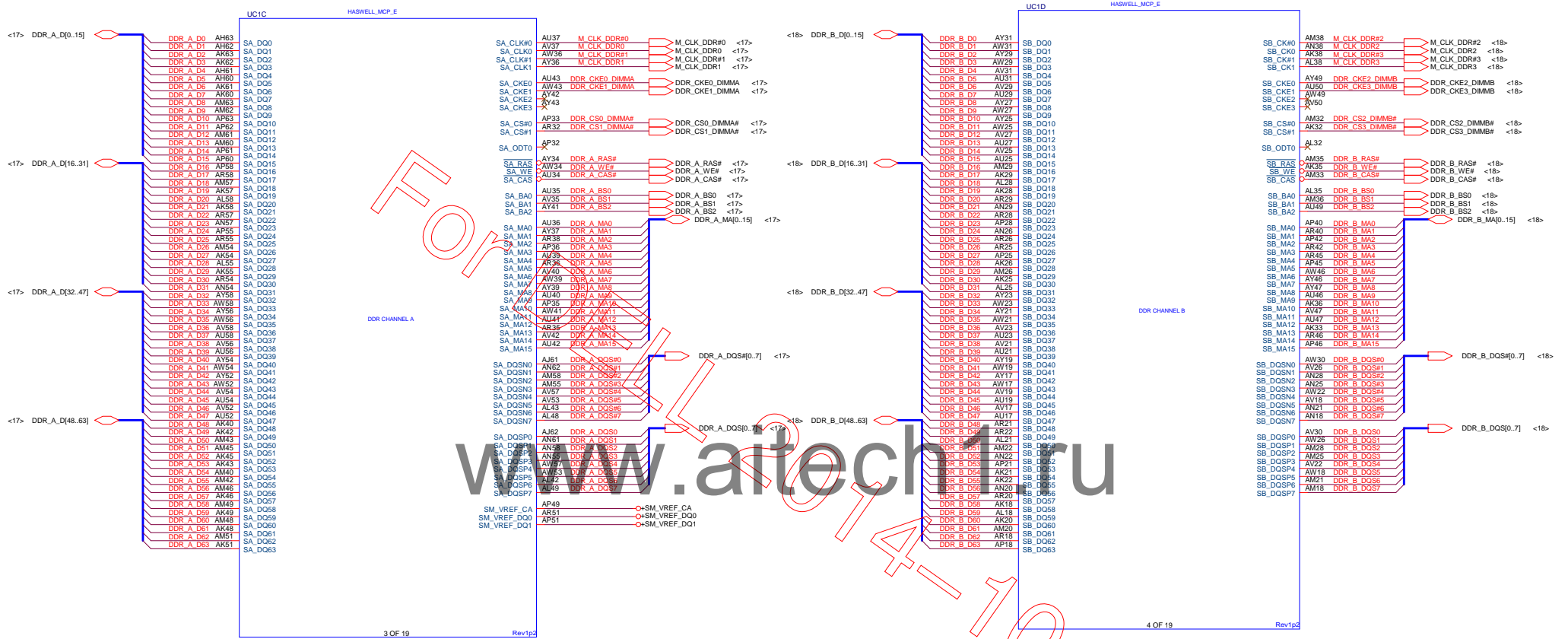


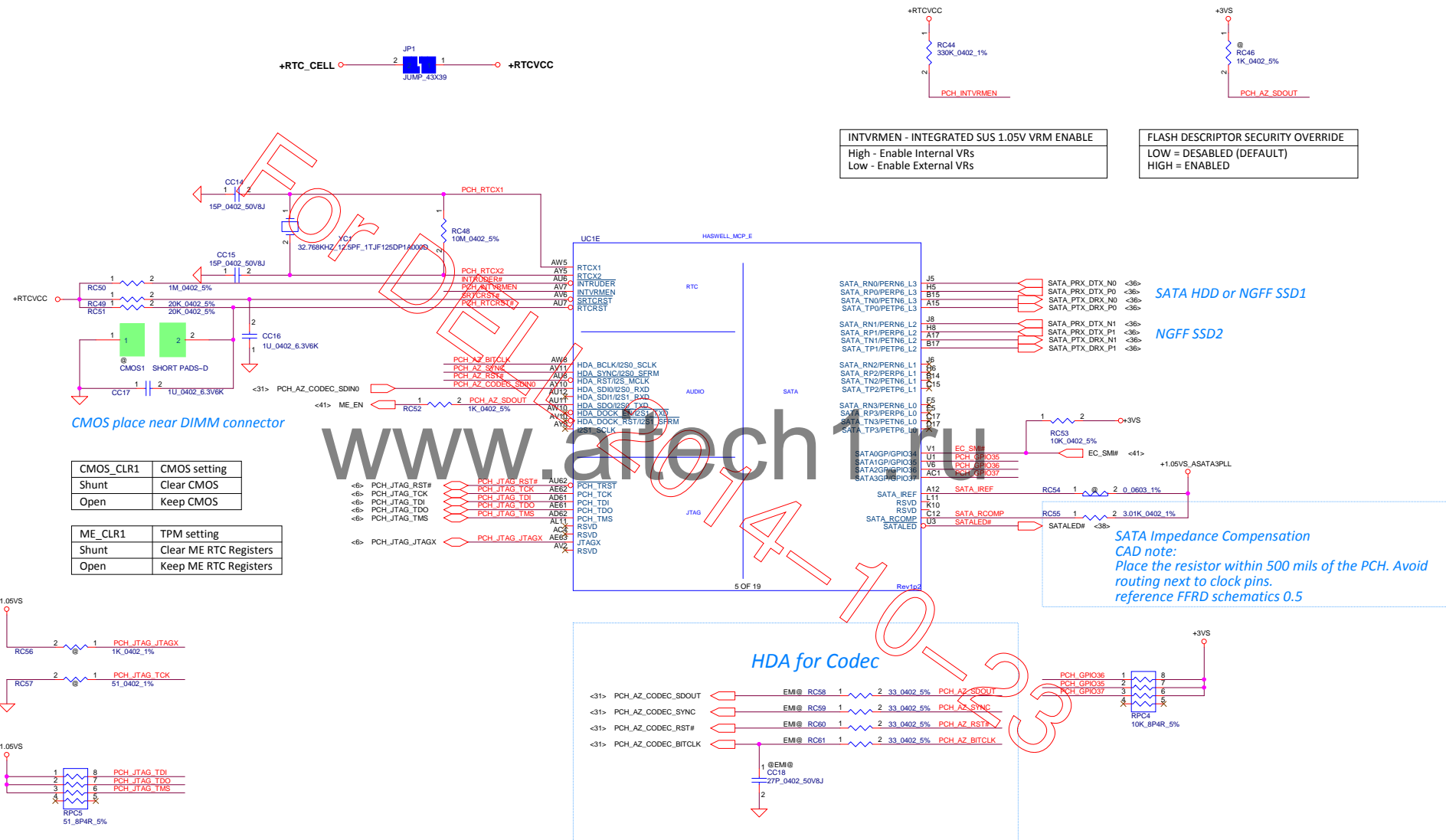




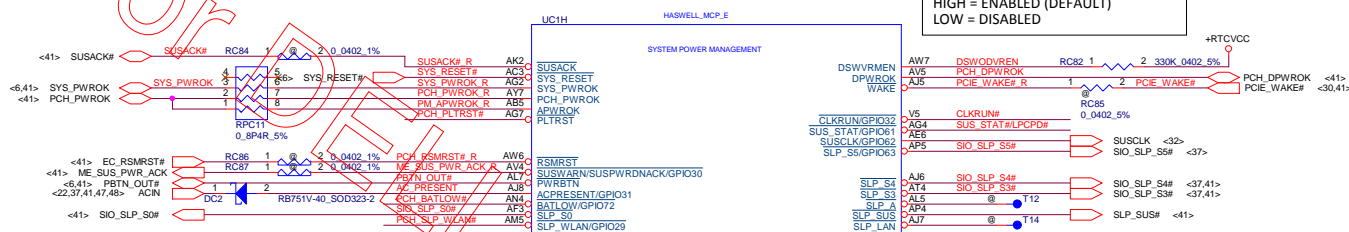
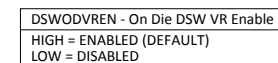
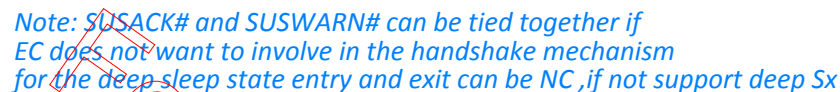
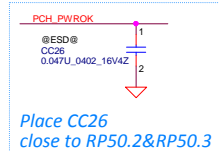
Security Classification	Compal Secret Data				Title		Compal Electronics, Inc.	
Issued Date	2013/09/09	Deciphered Date	2014/09/09		Size	MCP(1.2) vDP_XDP MISC		Rev. 1
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# Non-Interleaved memory

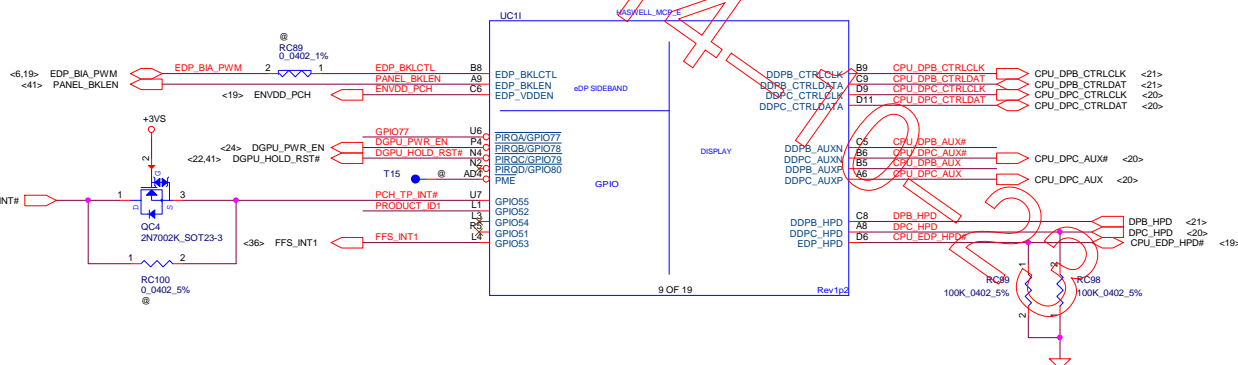




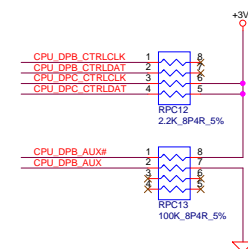




*PCH\_BATLOW# need pull high to VCCDSW3\_3  
(If no deep Sx, connect to VCCSUS3\_3)*



PRODUCT\_ID1:  
Haswell---H  
Broadwell---L



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					Size	Document Number	Rev
					LA-A30IP		
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PCIE 4X MUX

WLAN (M.2 Card)

10/100/1000 LAN

Left side 2

Caldera

Left side 1

Right side (power share)

Left side 2

Caldera

Touch screen

Camera

ELC

Bluetooth

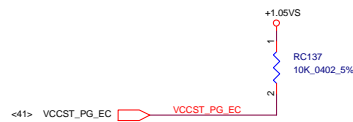
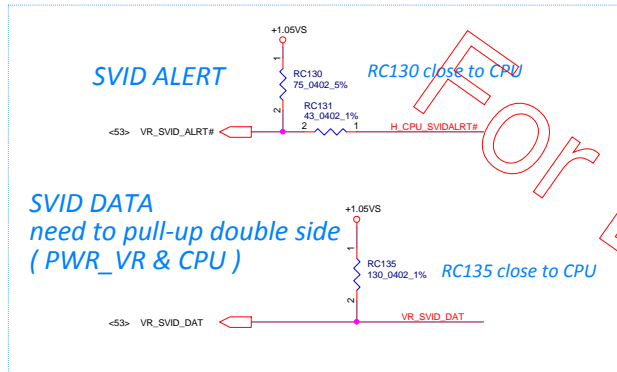
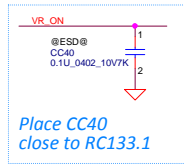
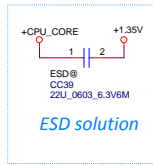
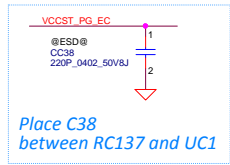
Left side 1

Right side (power share)

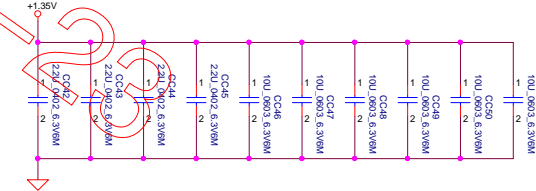
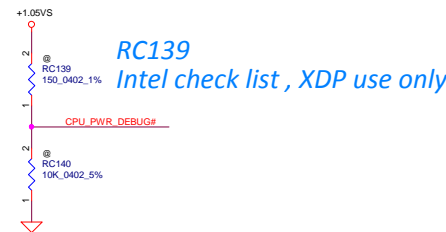
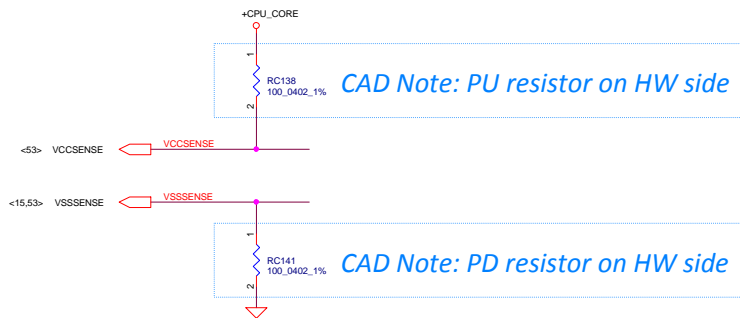
**CAD NOTE:**  
Route single-end 50-ohms and max 500-mils length.  
Avoid routing next to clock pins or under stitching capacitors.  
Recommended minimum spacing to other signal traces is 15 mils.

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				Date	Friday, September 18, 2014
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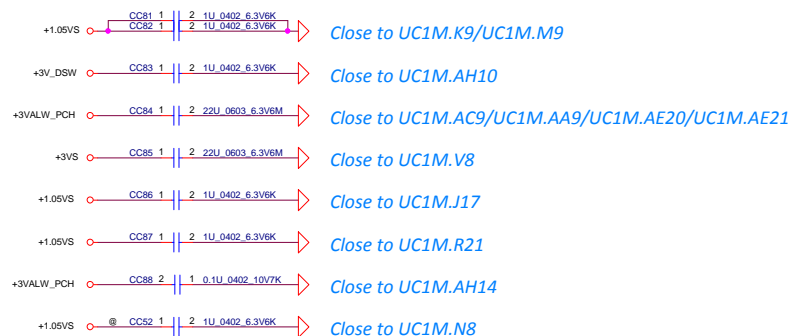
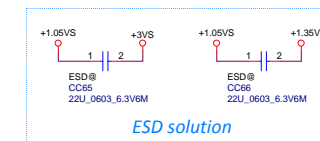
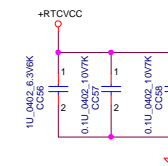
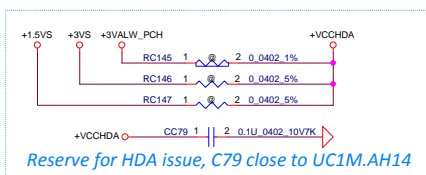


Define EC OD pin need double confirm.

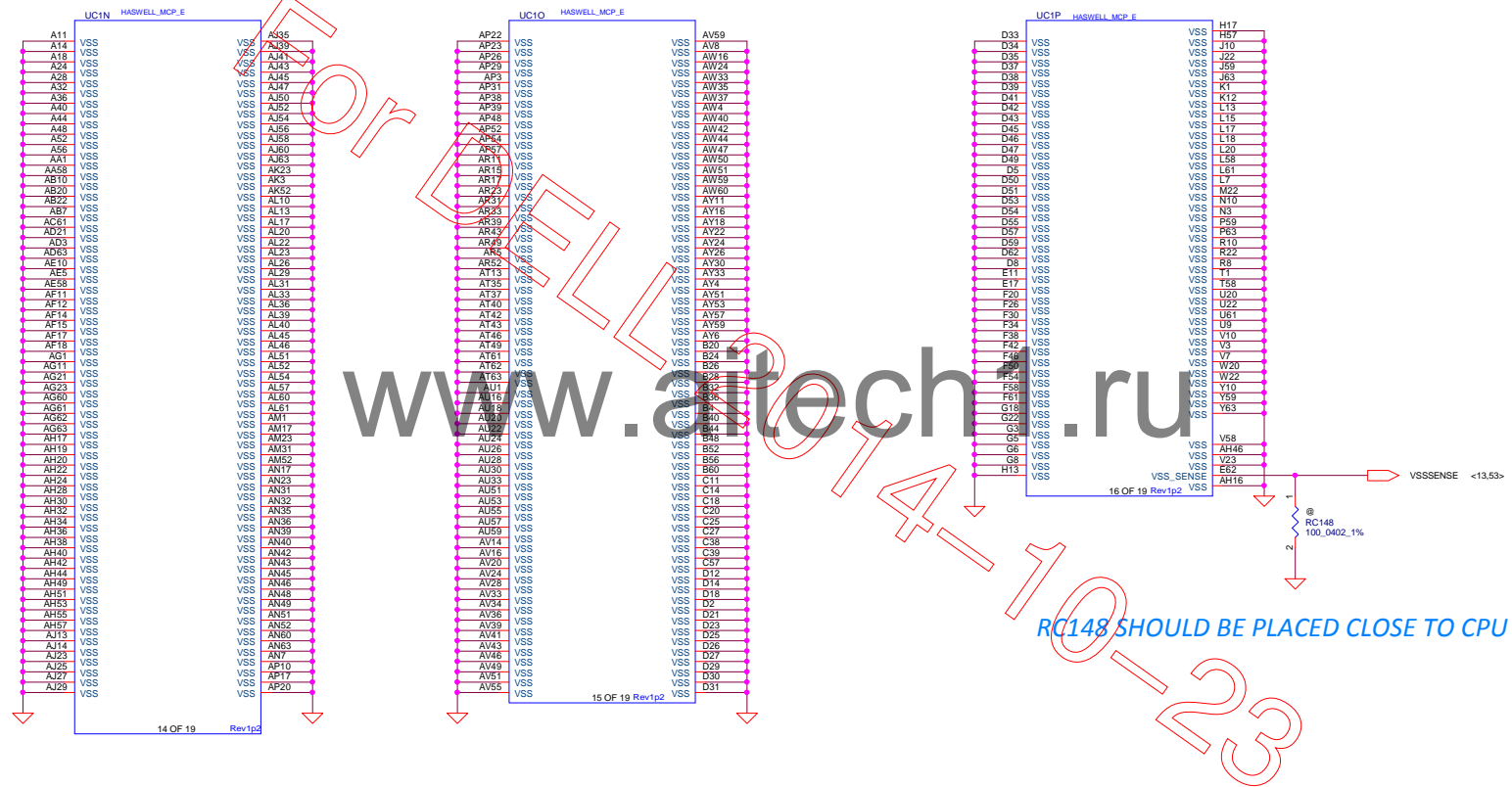


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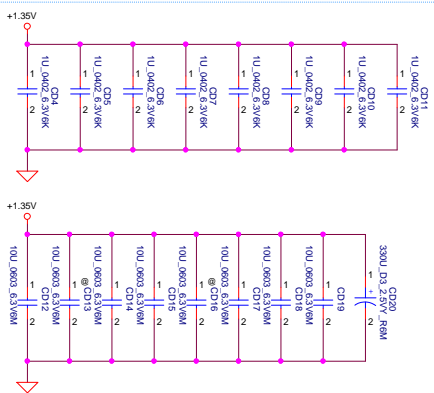
# 2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3  
VREFDQ multiple methods M1  
Populate RD7, De-Populate RD1 for Intel DDR3  
VREFDQ multiple methods M3

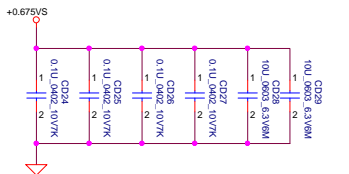
<7> DDR\_A\_DQS#0..7  
<7> DDR\_A\_DQ0..63  
<7> DDR\_A\_DQS0..7  
<7> DDR\_A\_MA0..15

All VREF traces should  
have 10 mil trace width  
Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket

CAD NOTE  
PLACE THE CAP NEAR TO  
DIMM RESET PIN



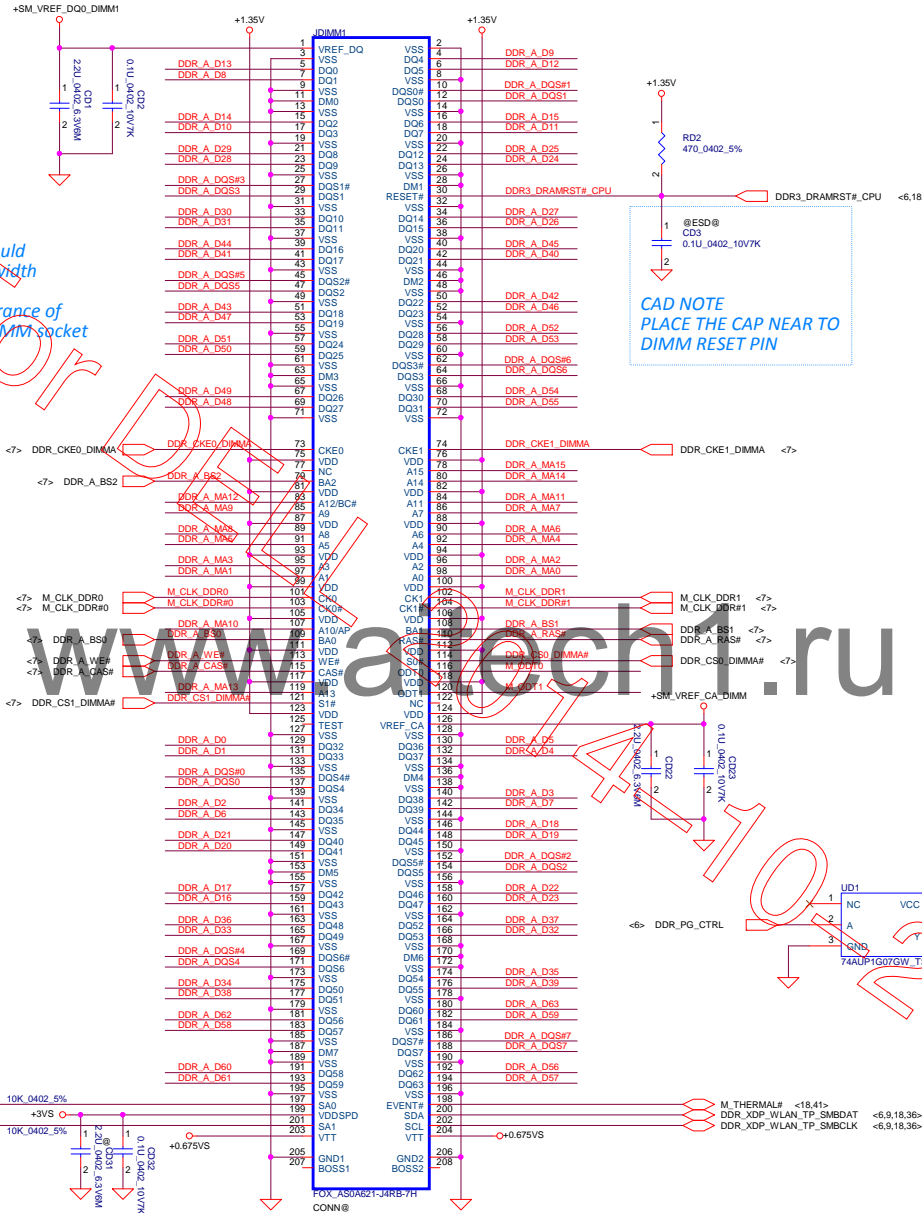
Layout Note:  
Place near JDIMM1



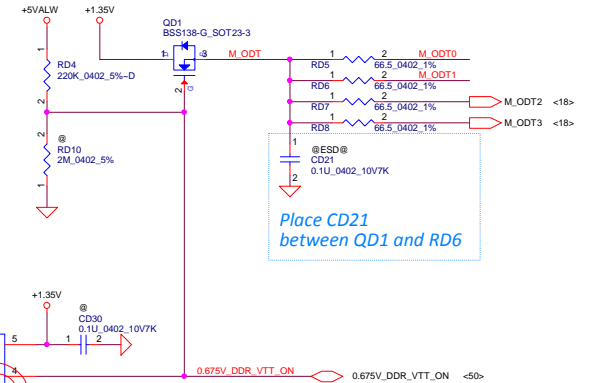
Layout Note:  
Place near JDIMM1.203,204



ESD solution



## DDR3L SODIMM ODT GENERATION



Place CD21  
between QD1 and RD6

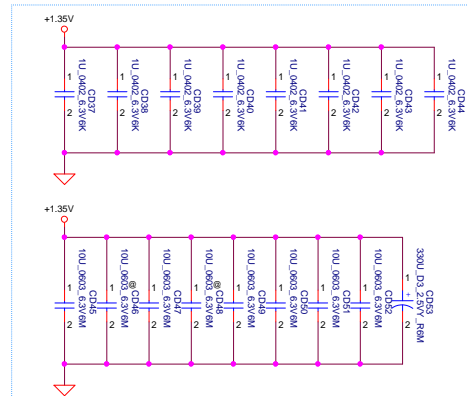
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# 2-3A to 1 DIMMs/channel

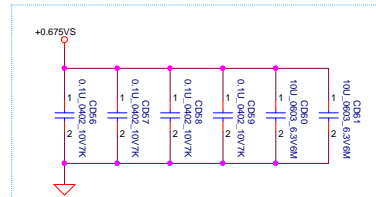
Populate RD13, De-Populate RD8 for Intel DDR3  
VREFDQ multiple methods M1  
Populate RD8, De-Populate RD13 for Intel DDR3  
VREFDQ multiple methods M3

<7> DDR\_B\_DQS#0..7  
<7> DDR\_B\_DQ0..63  
<7> DDR\_B\_DQS#0..7  
<7> DDR\_B\_MA0..15

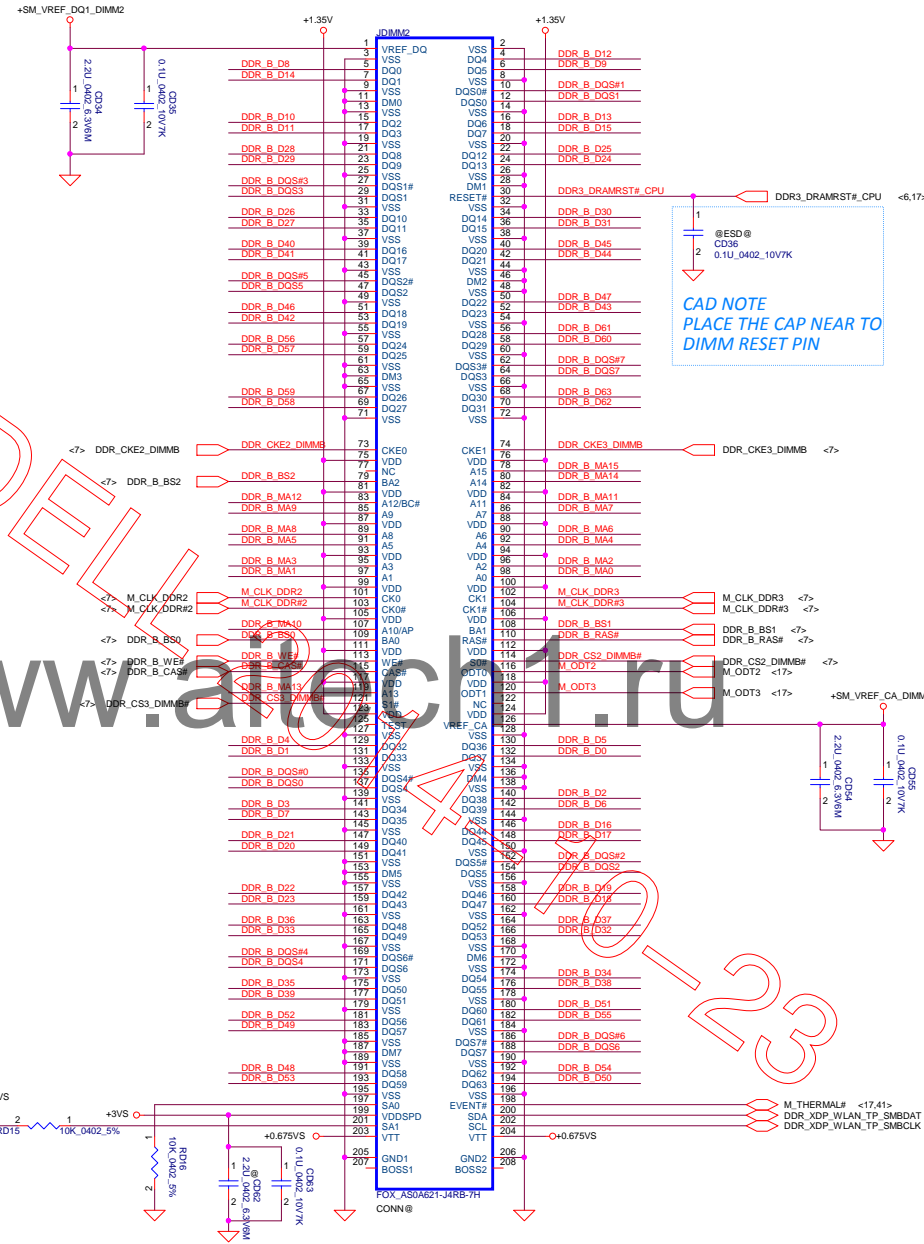
All VREF traces should  
have 10 mil trace width  
Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



Layout Note:  
Place near JDIMM2

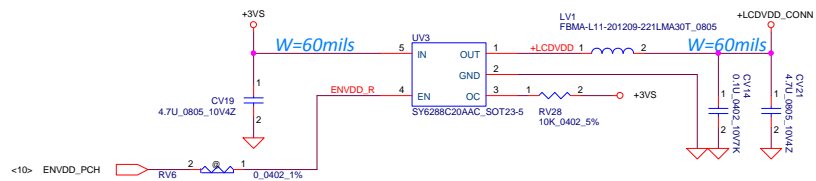


Layout Note:  
Place near JDIMM2.203,204

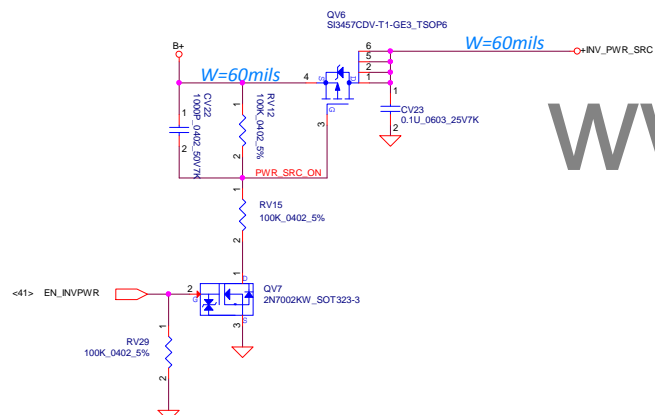


CAD NOTE  
PLACE THE CAP NEAR TO  
DIMM RESET PIN

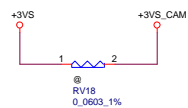
## LCD power control



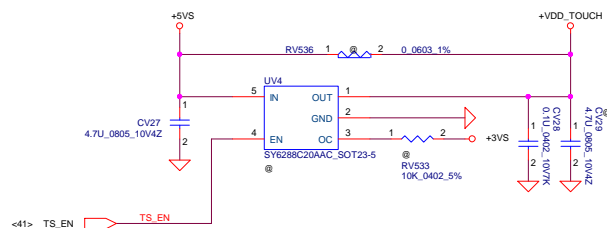
## LCD backlight power control



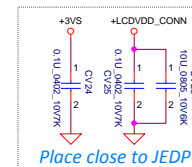
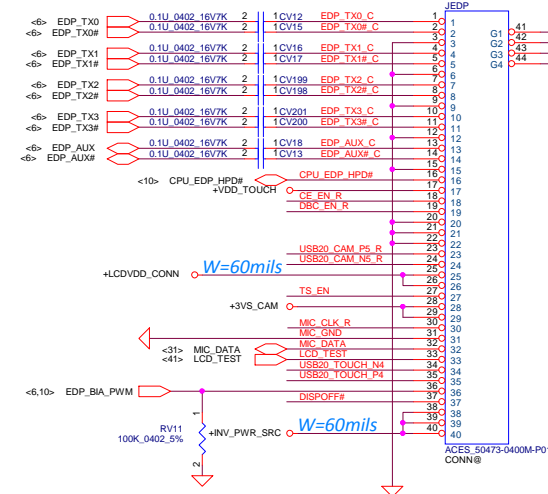
## Webcam power control



## Touch screen panel power control

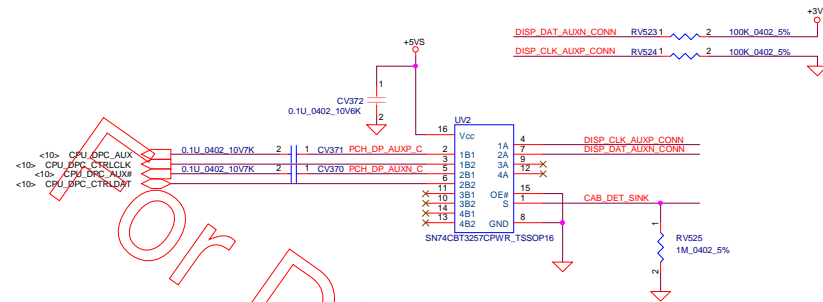


## eDP connector



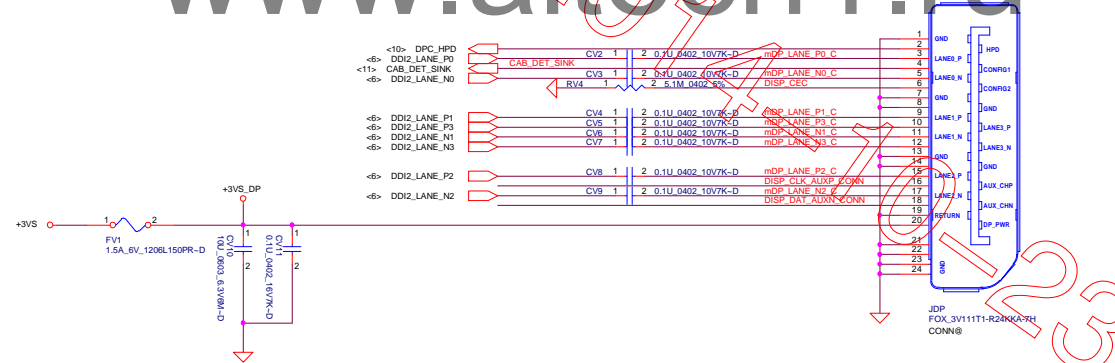
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2013/09/09		2014/09/09		eDP/webcam/touch	
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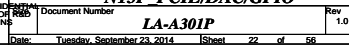
S = L, A port = B1 port (DP Port)  
S = H, A port = B2 port (HDMI/DVI/VGA Dongle)

www.aitech1.ru Mini DP connector

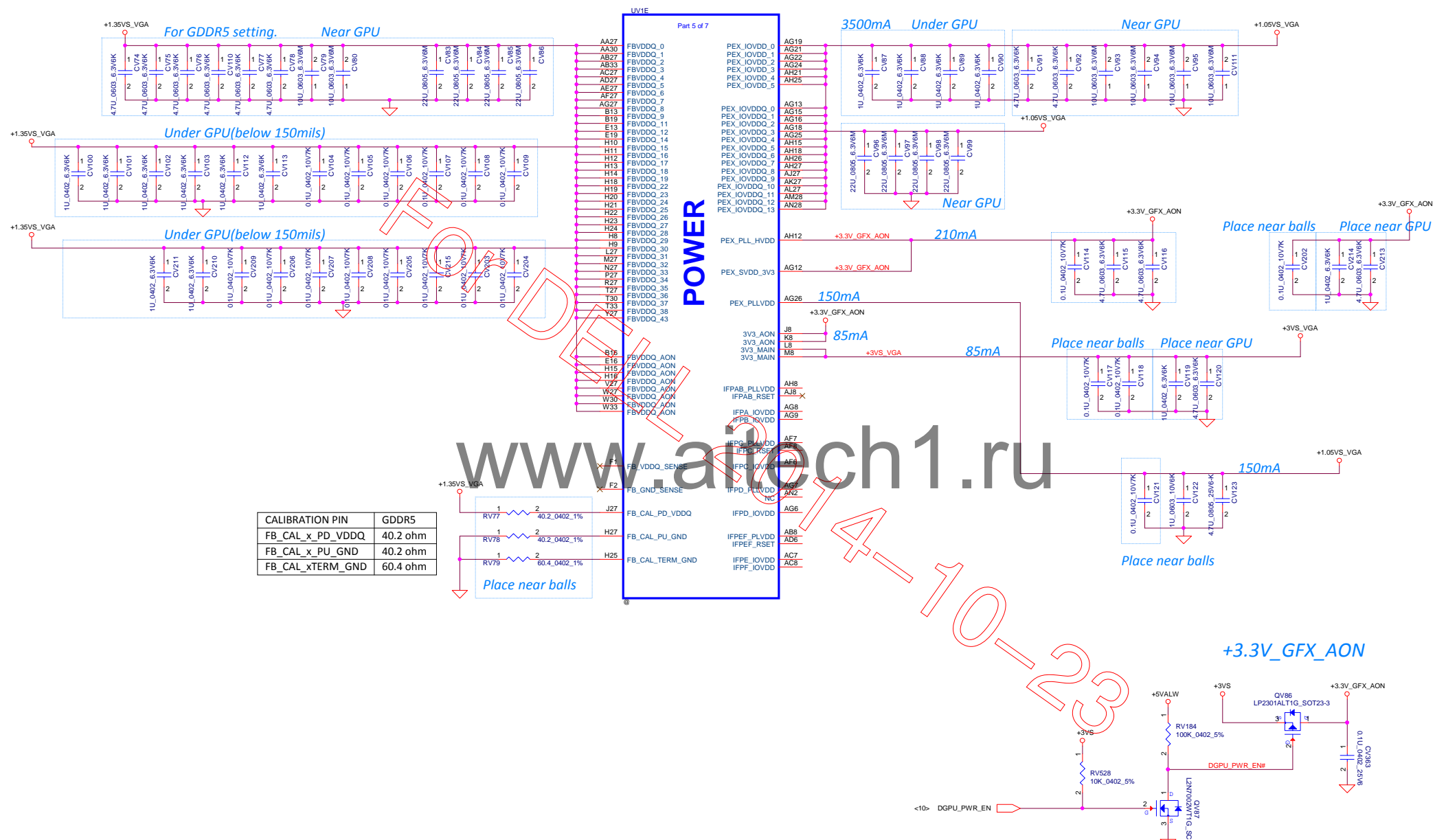






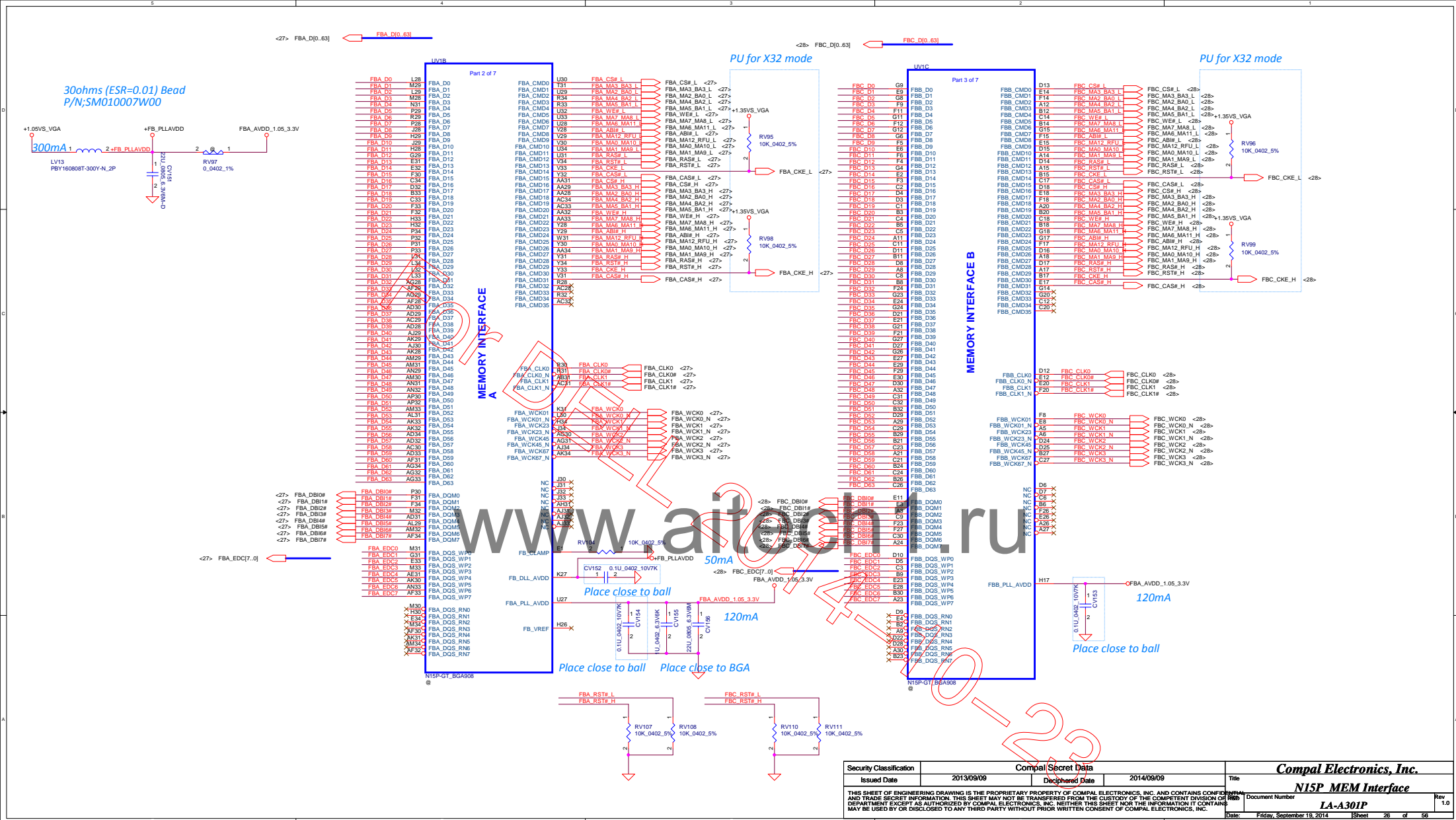






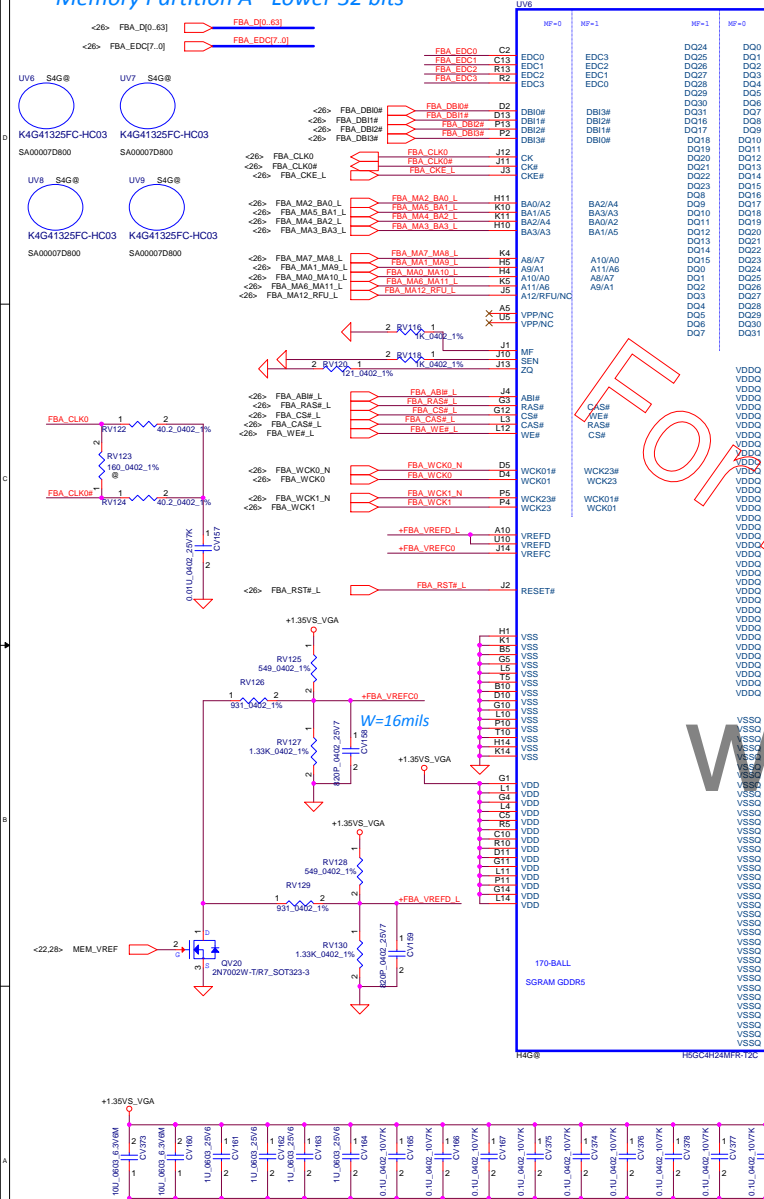
CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm



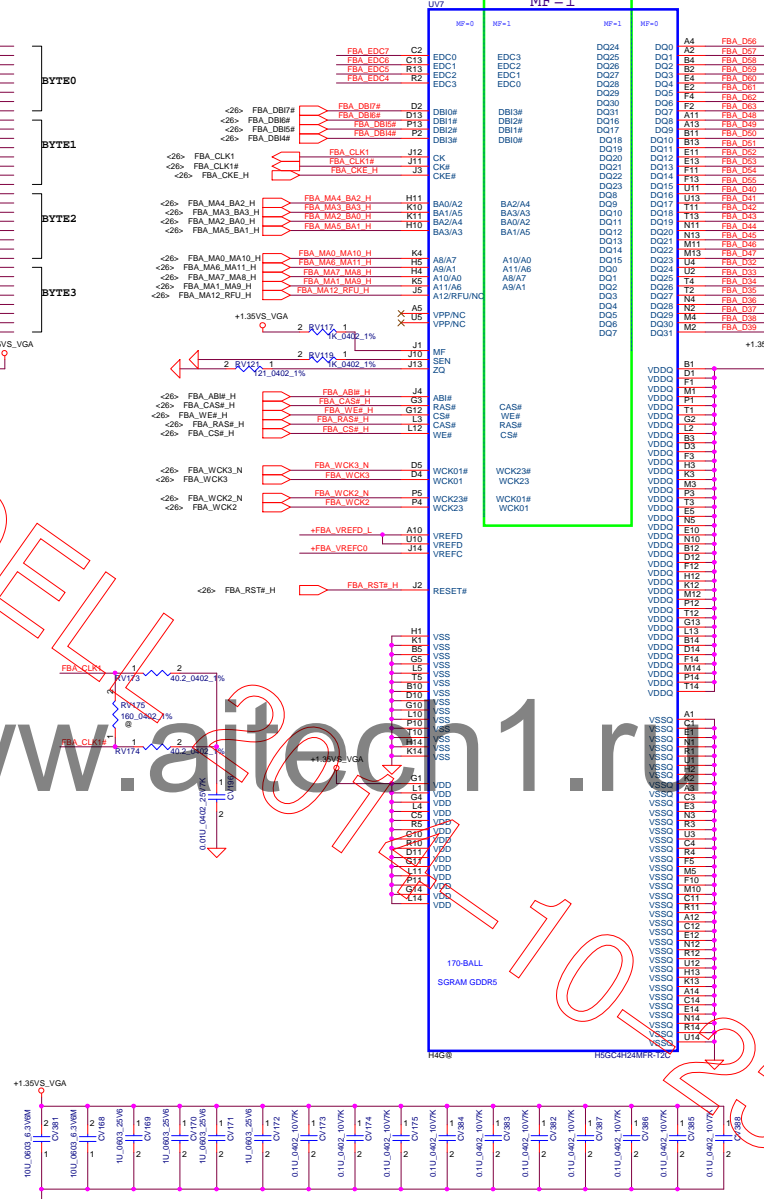


# Memory Partition A - Lower 32 bits

MF=0



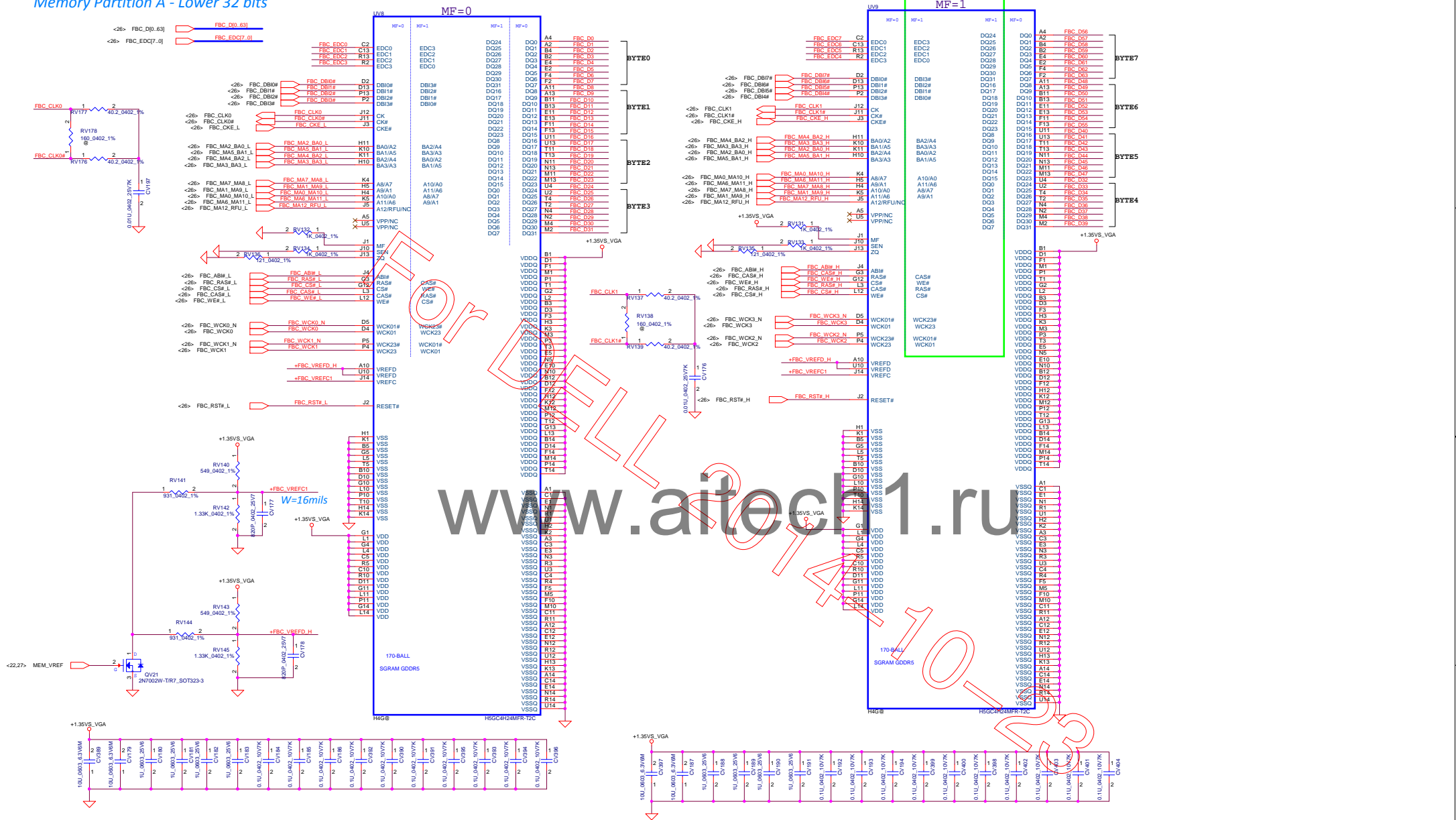
MF=1



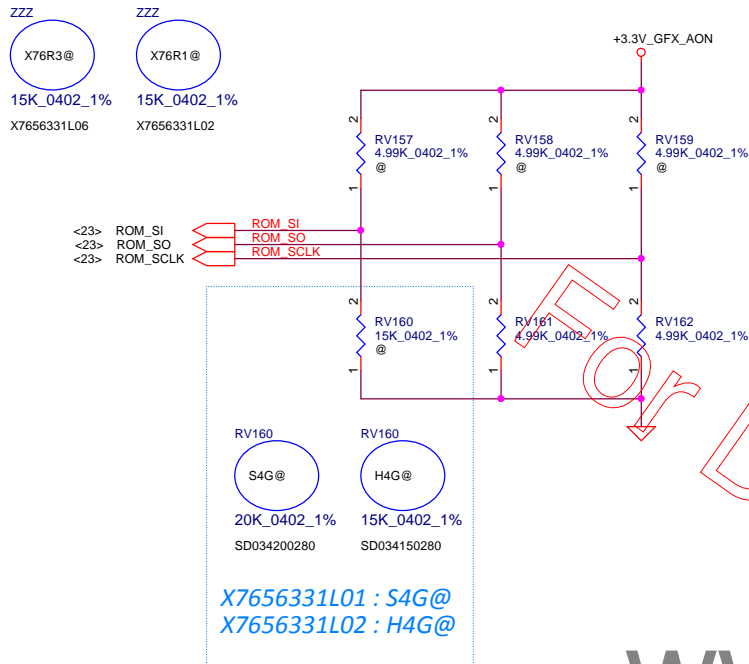
Security Classification		Compal Secret Data	
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Title		N1SP_GDDR5_A	
Size	Document Number	LA-A301P	
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Memory Partition A - Lower 32 bits



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Date:	Friday, September 19, 2014	Sheet	28	of 56

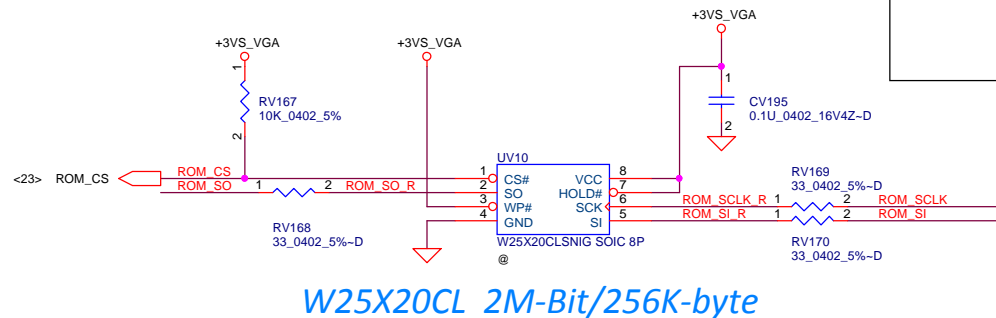


SA00007D800 S IC D5 128M32 K4G41325FC-HC03 FBGA 170P

SA00006040L S IC D5 128M32/2.5G H5GC4H24MFR-T2C FBGA

SA00006041L S IC D5 128M32/2.5G H5GC4H24MFR-T2C A31!

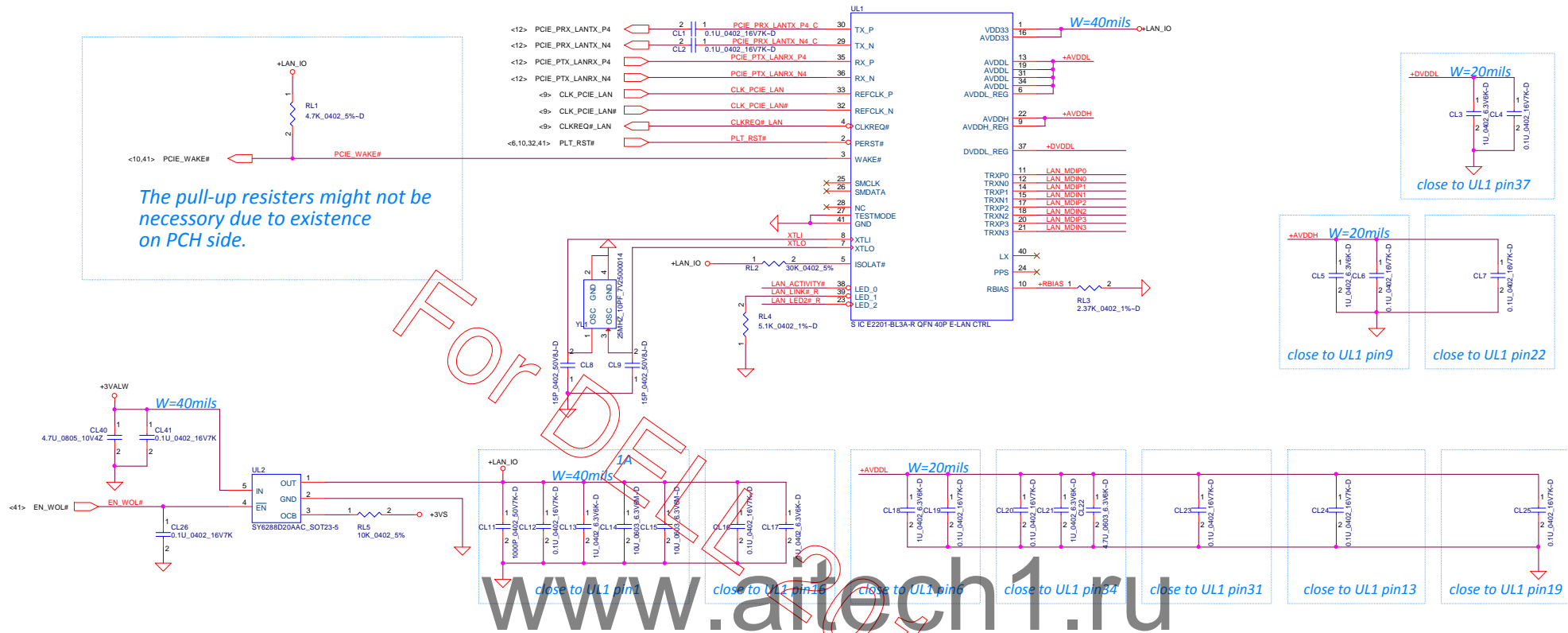
GPU	FB Memory	DDR5	ROM_SO	ROM_SCLK	ROM_SI	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15P-GX	Samsung	2500MHz	PD	PD	PD	PU	PD	PD	PD	PD
		K4G41325FC-HC03								
		256Mx16								
	Hynix	2500MHz	PD	PD	PD	PU	PD	PD	PD	PD
		H5GC4H24MFR-T2C								
		256Mx16								



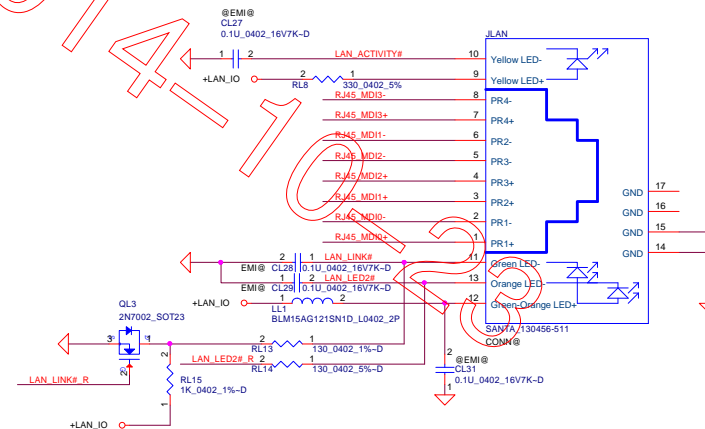
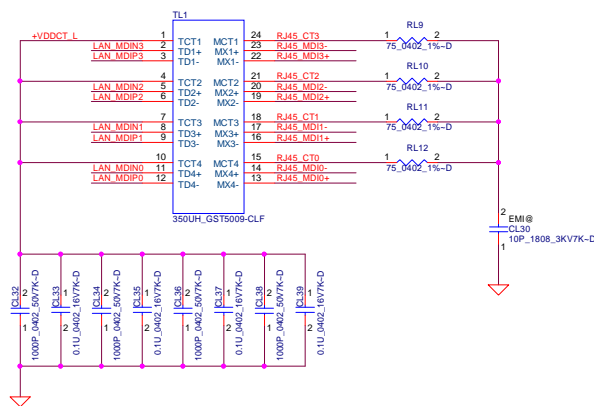
W25X20CL 2M-Bit/256K-byte

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					Custom	LA-A301P		
					Date:	Wednesday, September 24, 2014	Sheet	29 of 56

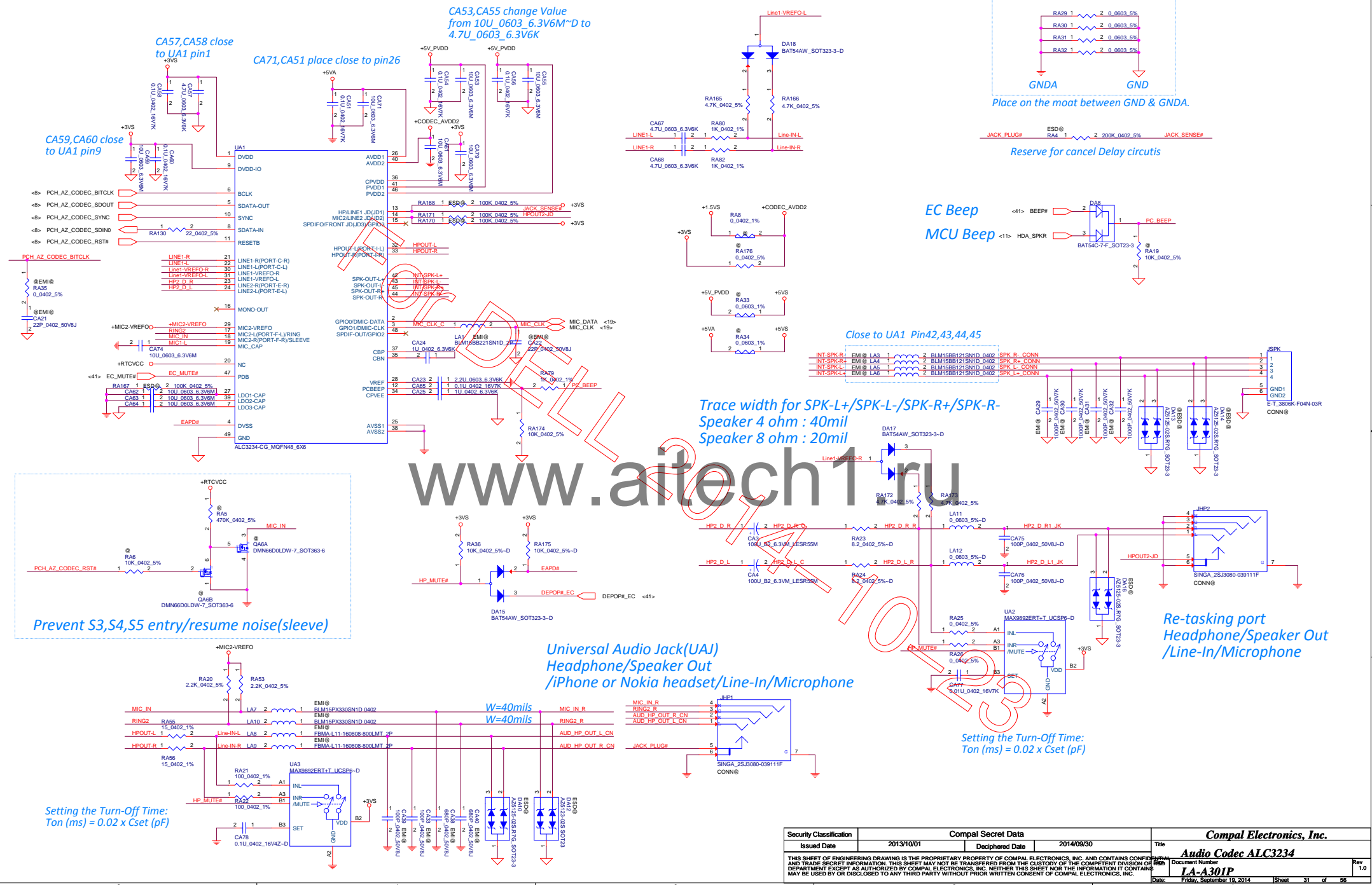




TIMAG: S X'FORM\_IH-160 LAN,SP050006F00  
 BOTHHAND: S X'FORM\_GST5009-D LF LAN,SP050006B00

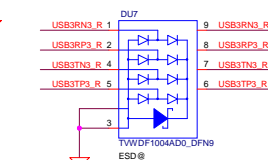


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From CPU RX

Pin Number	HD3SS3415	PI3PCIE3415
21	NC	VDD
25	NC	GND
31	NC	VDD
35	NC	GND
39	NC	VDD

From CPU TX

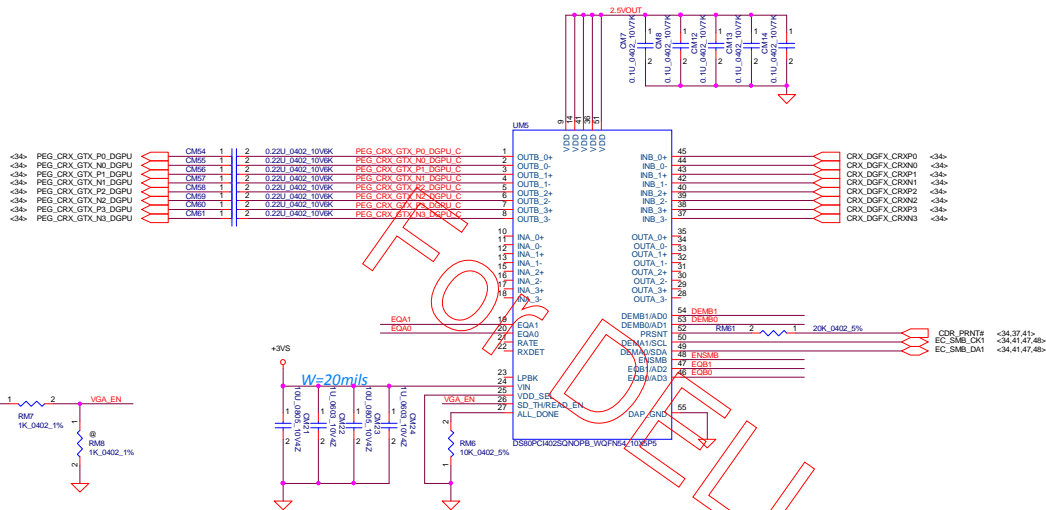
To N15P-GX TX

To N15P-GX RX

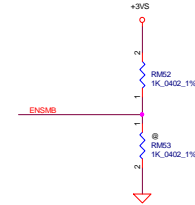
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PCIE\_CLK\_BUFFER

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Tie 1KΩ to VDD = Register Access SMBus Slave mode  
 FLOAT = Read External EEPROM (Master SMBUS Mode)  
 Tie 1KΩ to GND = Pin Mode



#### EQ Settings

Level	EQA1 EQB1	EQA0 EQB0	dB at 2.5G	dB at 4G	Suggested Use
1	0	0	3.7	4.9	< 5 inch trace
2	0	R	5.8	7.9	5 inch 5-mil trace
3	0	F	7.7	9.9	5 inch 4-mil trace
4	R	1	8.9	11	10 inch 5-mil trace
5	R	0	11.2	14.3	10 inch 4-mil trace
6	R	R	11.4	14.6	15 inch 4-mil trace
7	R	F	13.5	17	20 inch 4-mil trace
8	R	1	15	18.5	25 to 30 inch 4-mil trace
9	F	0	12.8	18	30 inch 4-mil trace
10	F	R	17.4	22	35 inch 4-mil trace
11	F	F	19.7	24.4	10m, 30awg cable
12	F	1	21.1	25.8	
13	1	0	21.7	27.4	
14	1	R	23.5	29.0	10m - 12m cable
15	1	F	25.8	31.4	
16	1	1	27.3	32.7	

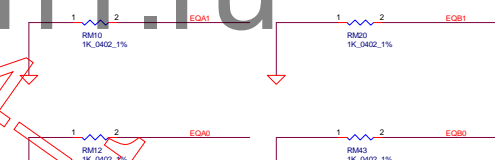
#### DEMA Settings

Level	DEMA1 DEMB1	DEMA0 DEMB0	DEMA DB	Suggested Use
1	0	0	0	< 5 inch 4-mil trace
2	0	R	0	< 5 inch 4-mil trace
3	0	F	-3.5	< 5 inch 4-mil trace
4	0	1	0	< 5 inch 4-mil trace
5	R	0	-3.5	10 inch 4-mil trace
6	R	R	-6	15 inch 4-mil trace
7	R	F	0	< 5 inch 4-mil trace
8	R	1	-3.5	10 inch 4-mil trace
9	F	0	-6	15 inch 4-mil trace
10	F	R	0	< 5 inch 4-mil trace
11	F	F	-3.5	10 inch 4-mil trace
12	F	1	-6	15 inch 4-mil trace
13	1	0	0	< 5 inch 4-mil trace
14	1	R	-3.5	10 inch 4-mil trace
15	1	F	-6	15 inch 4-mil trace
16	1	1	-9	20 inch 4-mil trace

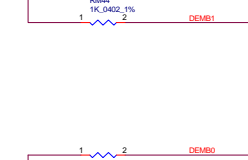
#### Level control Settings

Level	Pin Setting	Description	Suggested Use
1	0	1kΩ to GND	< 5 inch 4-mil trace
2	R	20KΩ to GND	< 5 inch 4-mil trace
3	F	Float	< 5 inch 4-mil trace
4	1	1kΩ to VDD	< 5 inch 4-mil trace

#### EQ\*MB



#### DEM\*EGPU

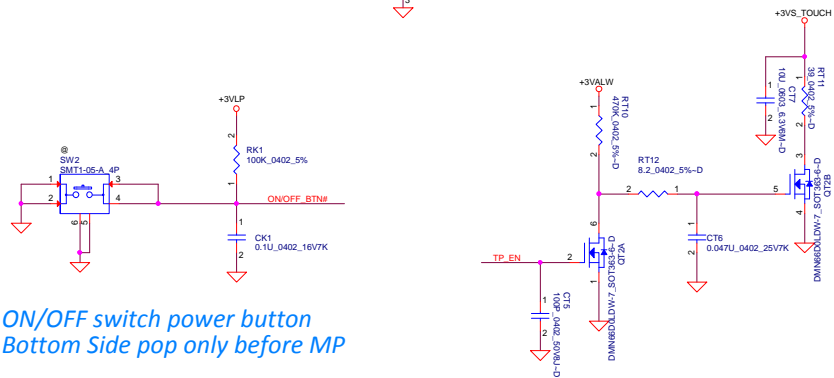
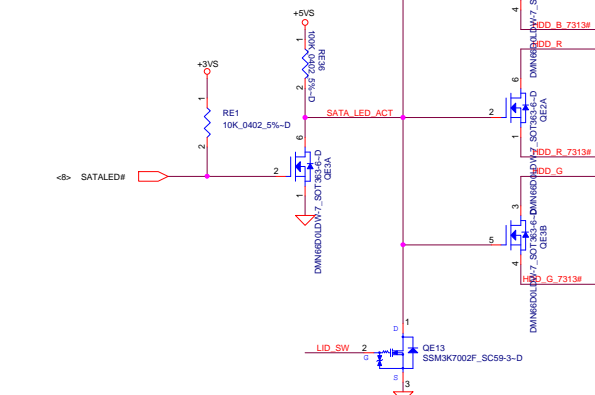
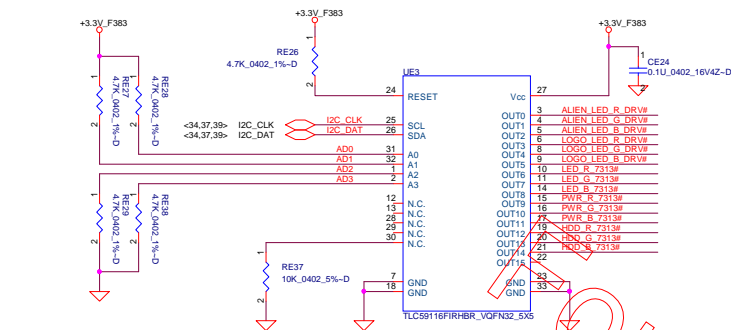


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Document Number				Rev
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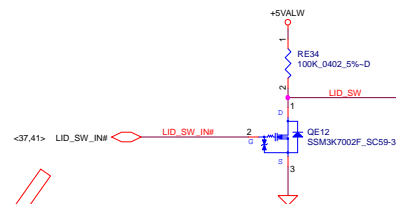
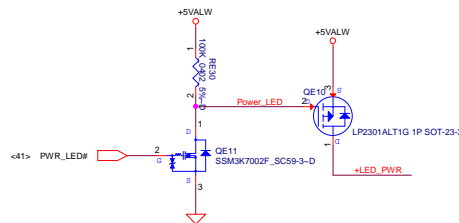




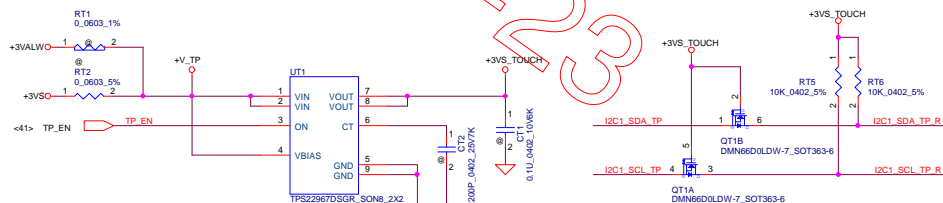


ON/OFF switch power button  
Bottom Side pop only before MP

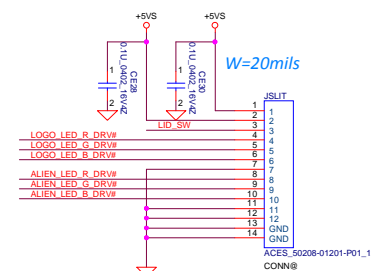
## Power LED



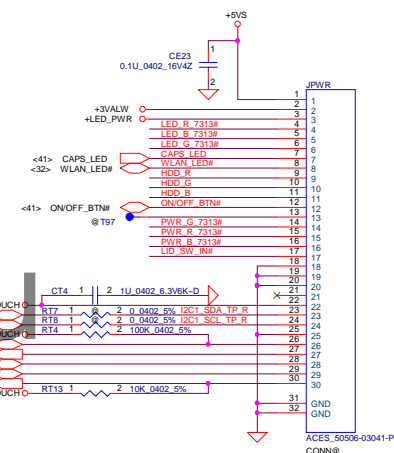
PTP pin define  
VDD  
I2C\_CLK  
I2C\_DAT  
GND  
ATTN  
PTP\_DISABLE#(CLOSE LID)  
PS2\_DATA  
PS2\_CLK  
PTP\_KBBL#(KB BL)  
NC



APE8937(SA000070L00)  
TPS22967(SA000070S00)



## Logic up LED board

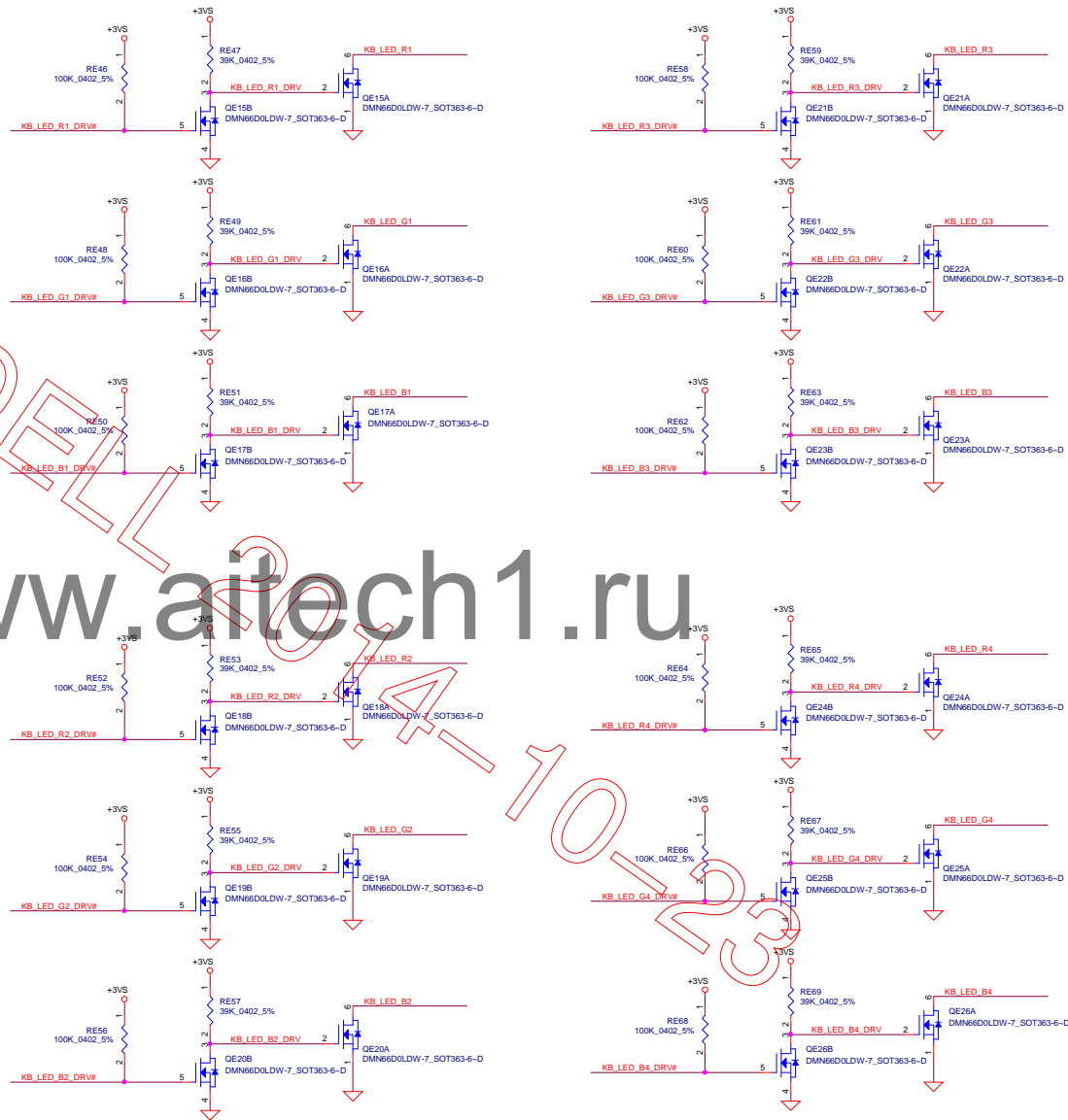
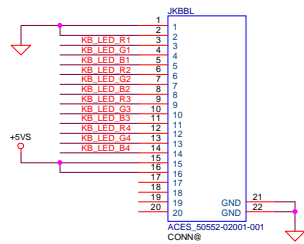
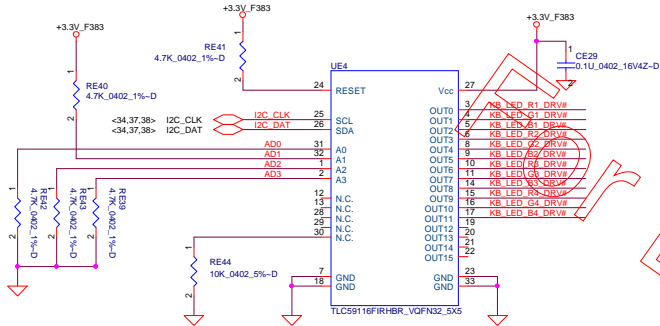


## Logic low LED board

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I2C address

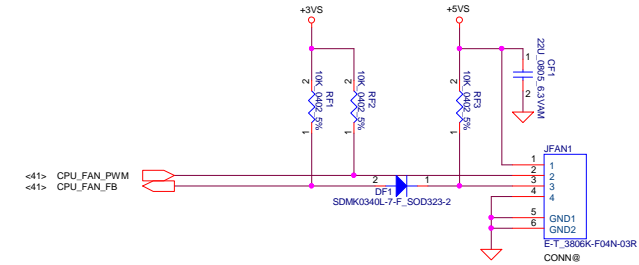
	A3	A2	A1	A0
UE1 (sheet 10 in Caldera board)	0	0	0	1
UE4 (sheet 39)	0	0	1	0
UE3 (sheet 38)	0	0	1	1
3rd LED drive (reserve)	0	1	0	0



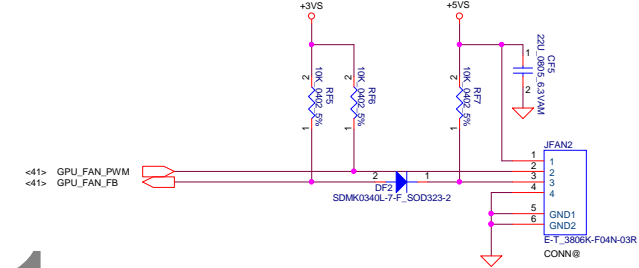
Diode circuit s used for skin temp sensor  
(placed near CPU).  
Place CF3 close to QF1 as possible.

Diode circuit s used for skin temp sensor  
(placed between DIMM1 and DIMM2).  
Place CF7 close to QF2 as possible.

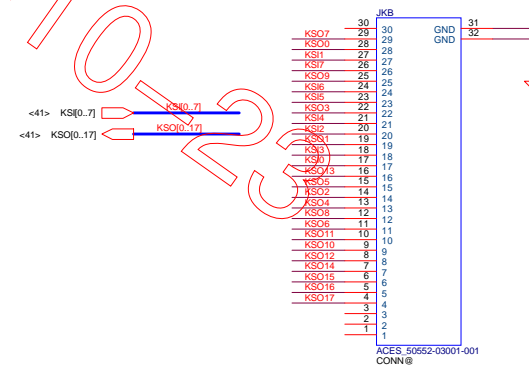
## CPU FAN control circuit



## GPU FAN control circuit



## INT\_KBD Connector



UF1  
NCT7718W(SA000067P00)Address:1001\_100xb(0x98h)  
ADM1032ARMZ-REEL(SA010320110)Address:100\_1100(0x4C)  
UF2  
W83L771AWG-2(SA00003PU00)Address:1001\_101xb(0x9Ah)  
ADM1032ARMZ-2R(SA010320120)Address:100\_1101(0x4D)

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Place CK8 close to RC13.1

Please close to EC

ME\_FWP PCH has internal 20K pulldown (suspend power rail)

Reserve for abnormal shutdown

Board ID

SD028000080 0\_0402\_5%  
SD034120280 12K\_0402\_1%  
SD034150280 15K\_0402\_1%  
SD028200280 20K\_0402\_1%  
SD034100300 27K\_0402\_1%  
SD034430280 43K\_0402\_1%  
SD034560280 56K\_0402\_1%  
SD034750280 75K\_0402\_1%  
SD034100380 100K\_0402\_1%  
SD034130380 130K\_0402\_1%  
SD034160380 160K\_0402\_1%  
SD034200380 200K\_0402\_1%  
SD000001B80 240K\_0402\_1%  
SD00000G280 270K\_0402\_1%  
SD034330380 330K\_0402\_1%  
SD028430380 430K\_0402\_1%

221 ohm for white LED  
316 ohm for red LED  
on dock cable side

Place CE12 between DK1 and RK14

Place CK13 between DK1 and UK1

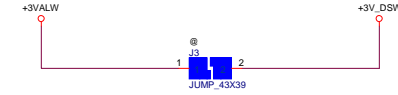
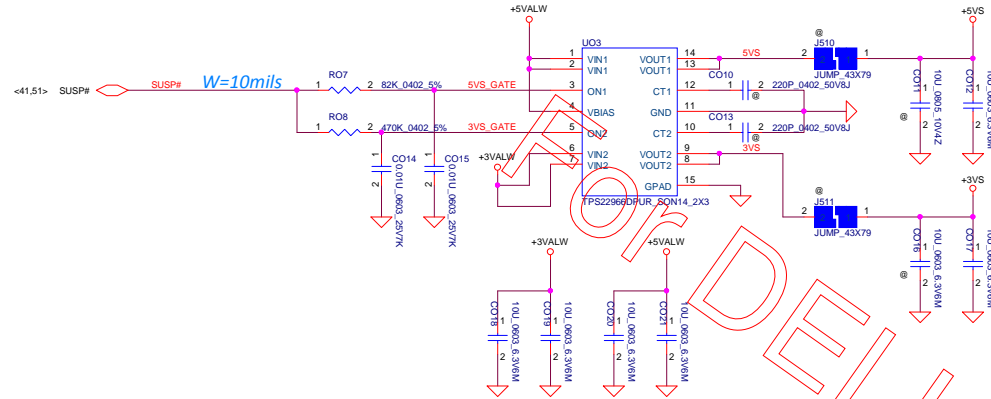
Place DK1 close to UK1

Place CK17, CK19, CK20 close to UK1

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		Date		Wednesday, September 24, 2014	
				Sheet 41 of 56	

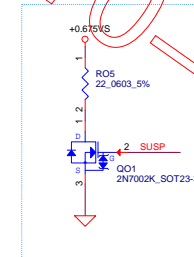
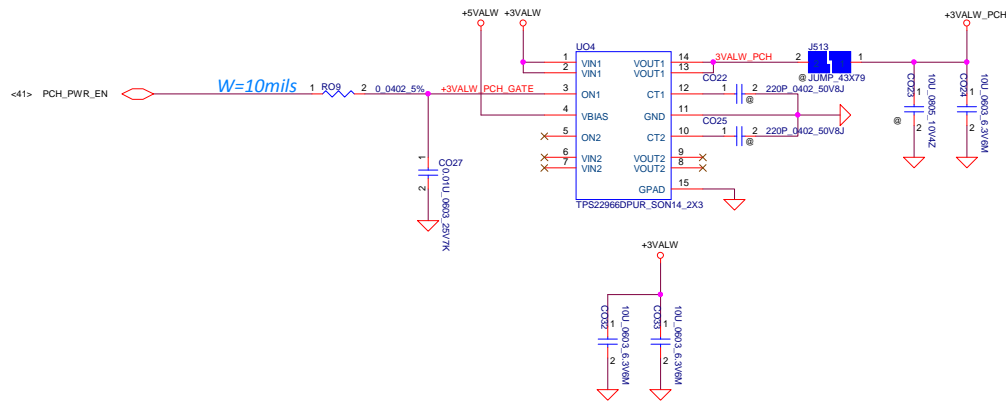
+5VS and +3VS switch

+3VALW TO +3V\_DSW

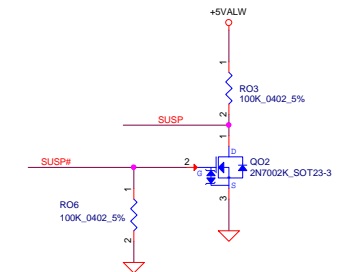


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+3VALW\_PCH switch

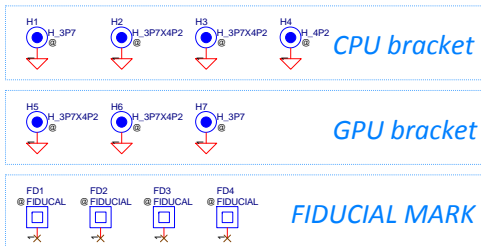
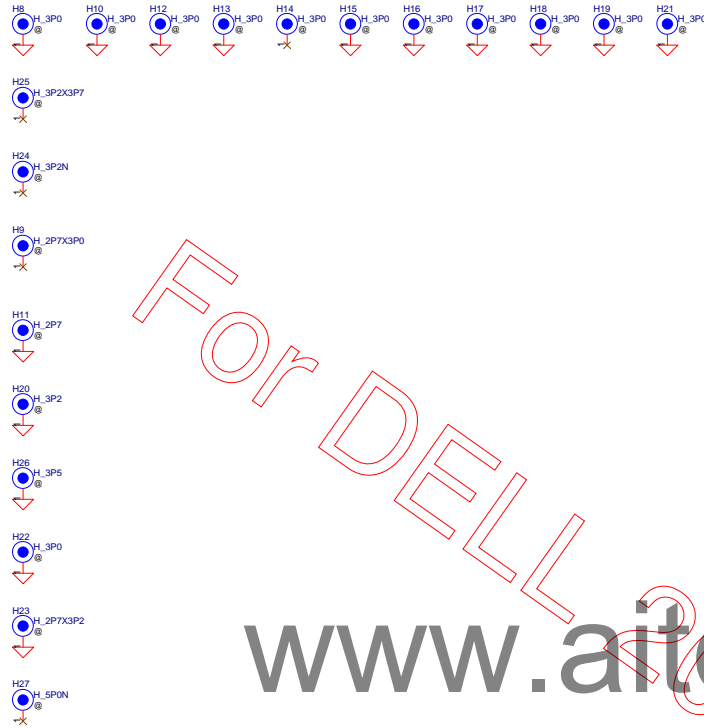


For Intel S3 power reduction

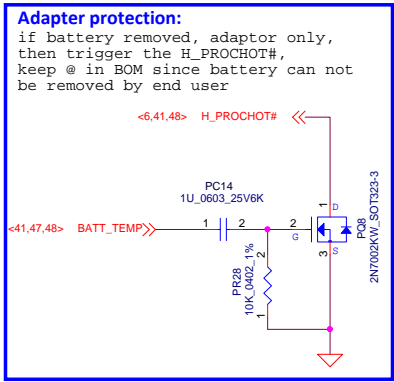
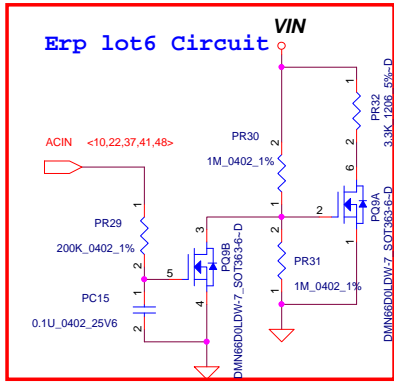
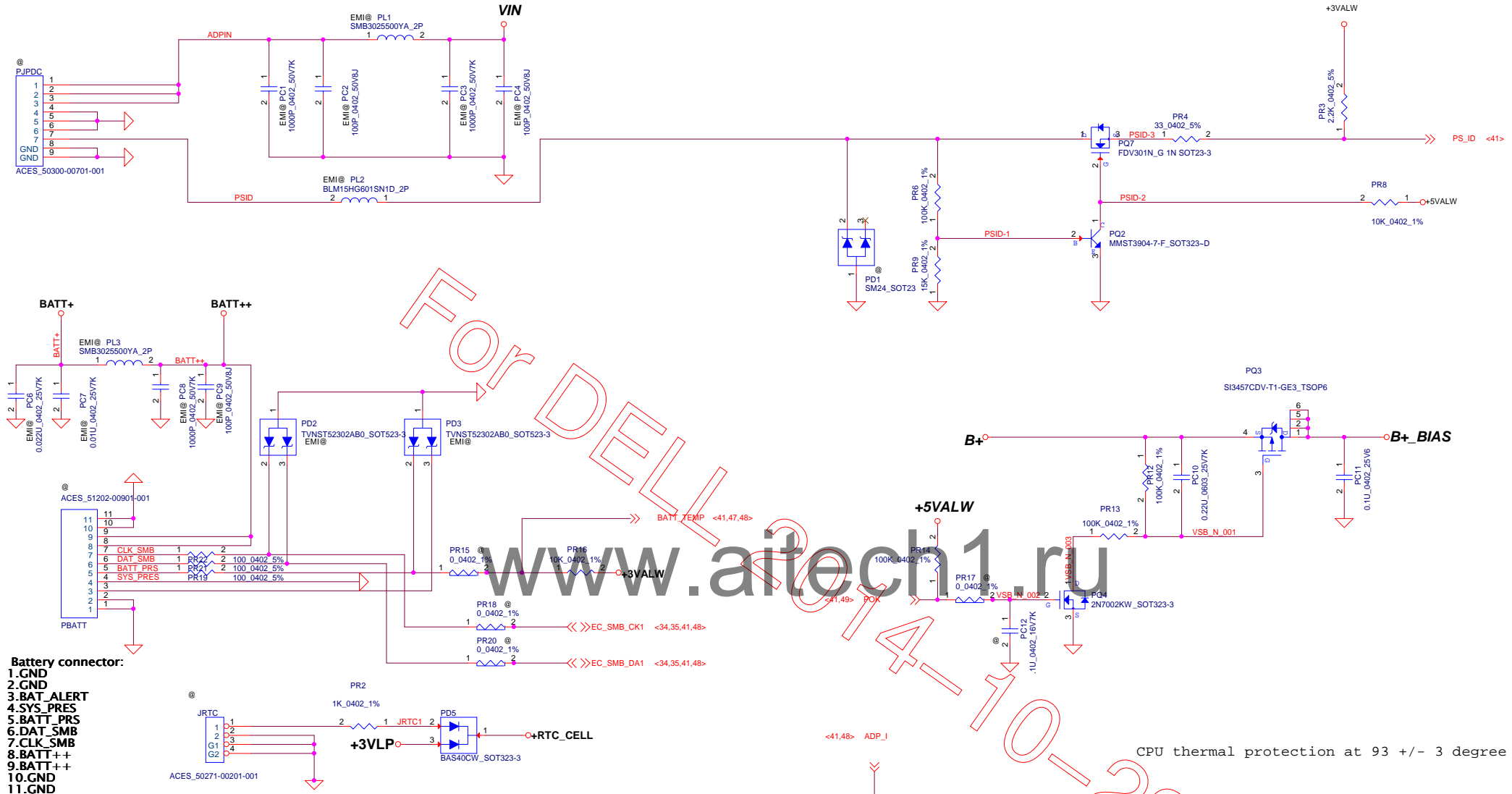


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# Screw Hole



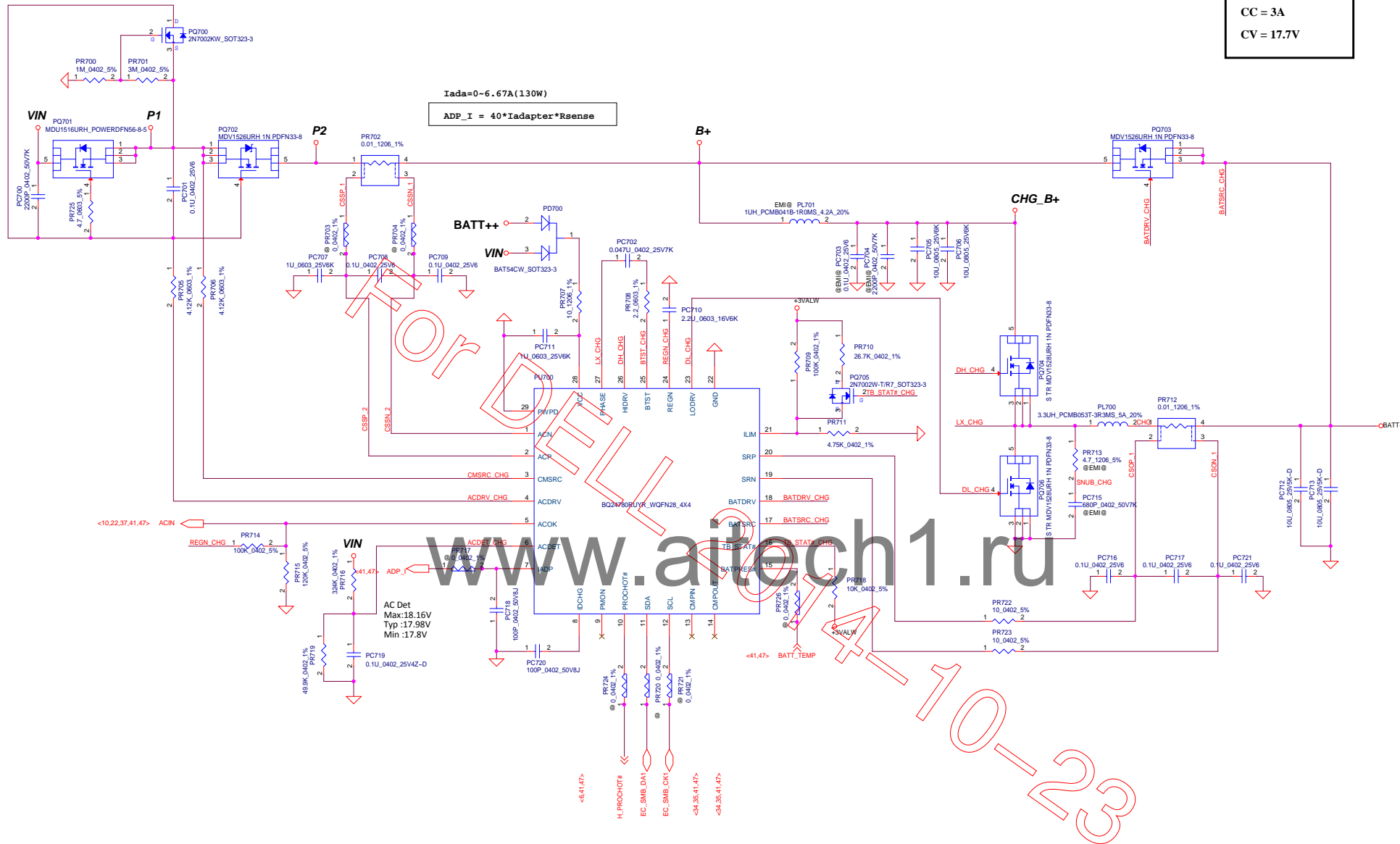
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Issued Date	2013/09/09	Deciphered Date	2014/09/09	Title		
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CC = 3A  
CV = 17.7V



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Issued Date	2013/09/09	Deciphered Date	2014/09/09	Title <b>PWR-Charger</b>	
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1.35VP  
TDC=16.7A  
Ipeak=24A  
OCP=28.8A  
Switching Frequency: 285kHz

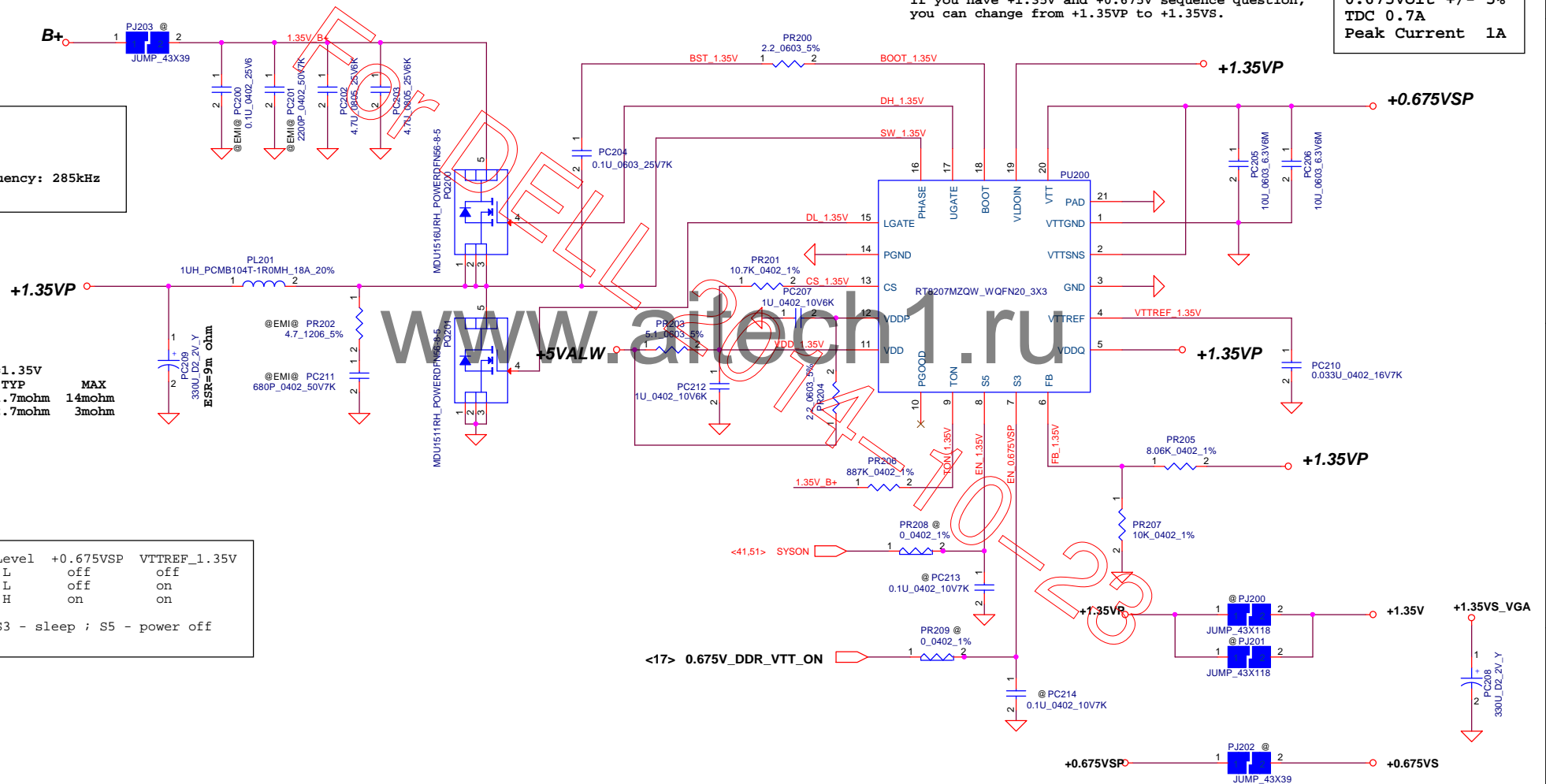
OVP: 110%~120%  
VFB=0.75V, Vout=1.35V  
TYP  
H/S Rds(on) : 11.7mohm 14mohm  
L/S Rds(on) : 2.7mohm 3mohm

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Pin19 need pull separate from +1.35VP.  
If you have +1.35V and +0.675V sequence question,  
you can change from +1.35VP to +1.35VS.

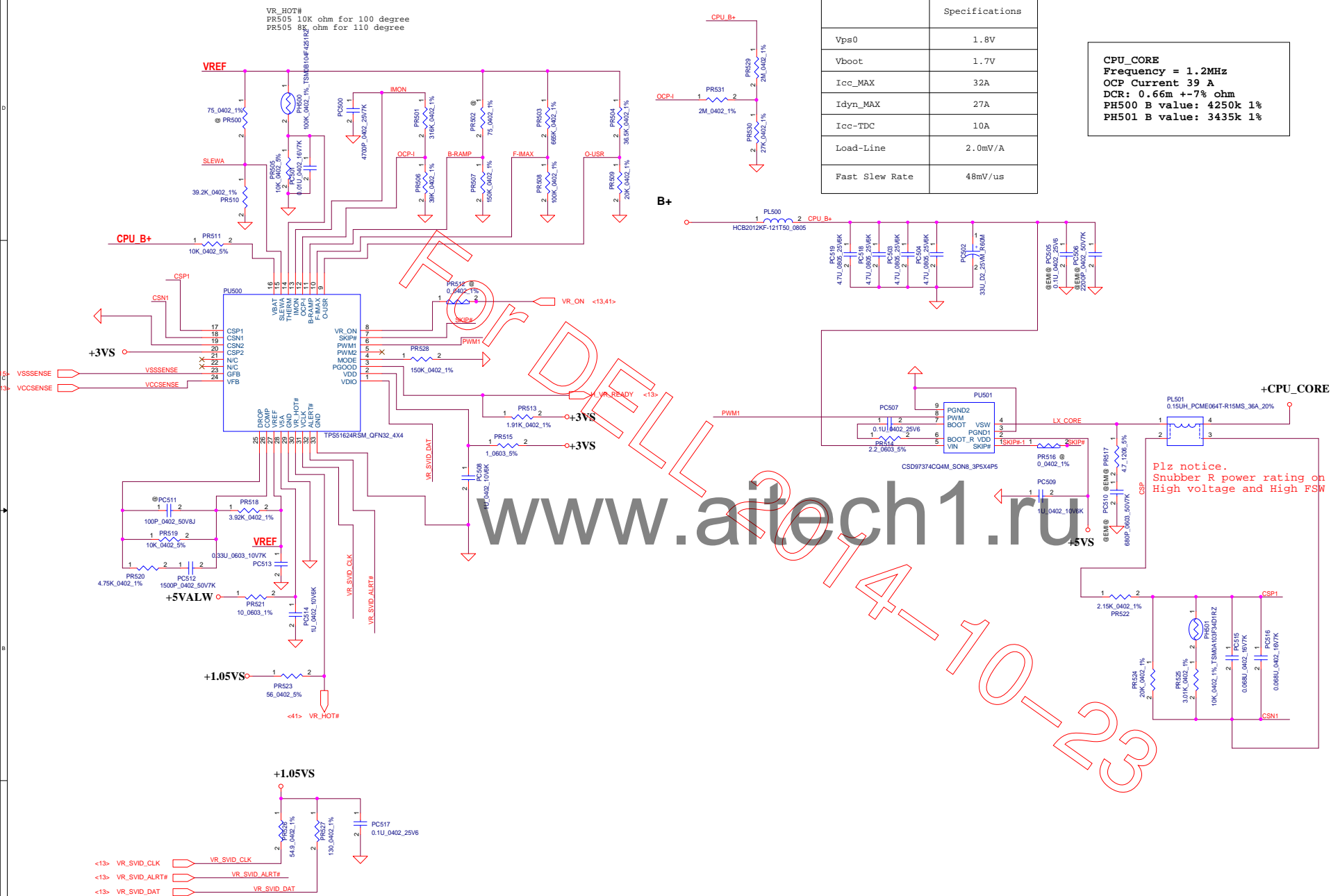
0.675Volt +/- 5%  
TDC 0.7A  
Peak Current 1A



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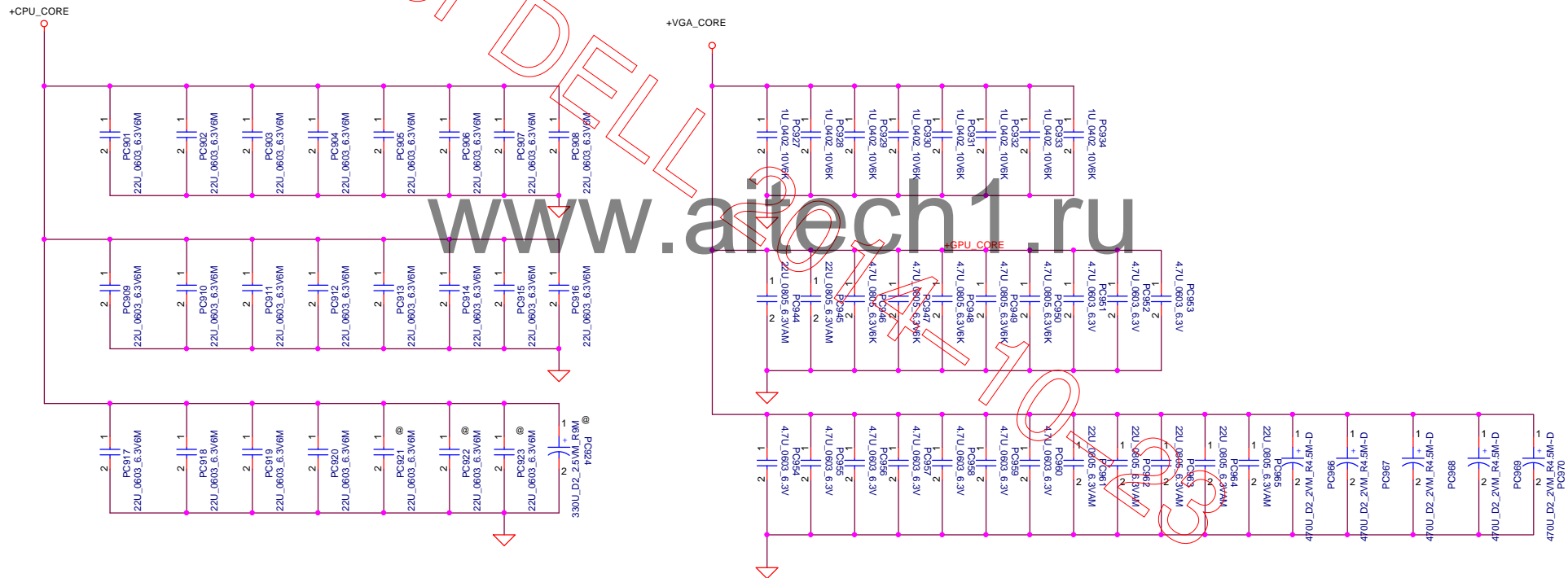






	Specifications
Vps0	1.8V
Vboot	1.7V
Icc_MAX	32A
Idyn_MAX	27A
Icc-TDC	10A
Load-Line	2.0mV/A
Fast Slew Rate	48mV/us

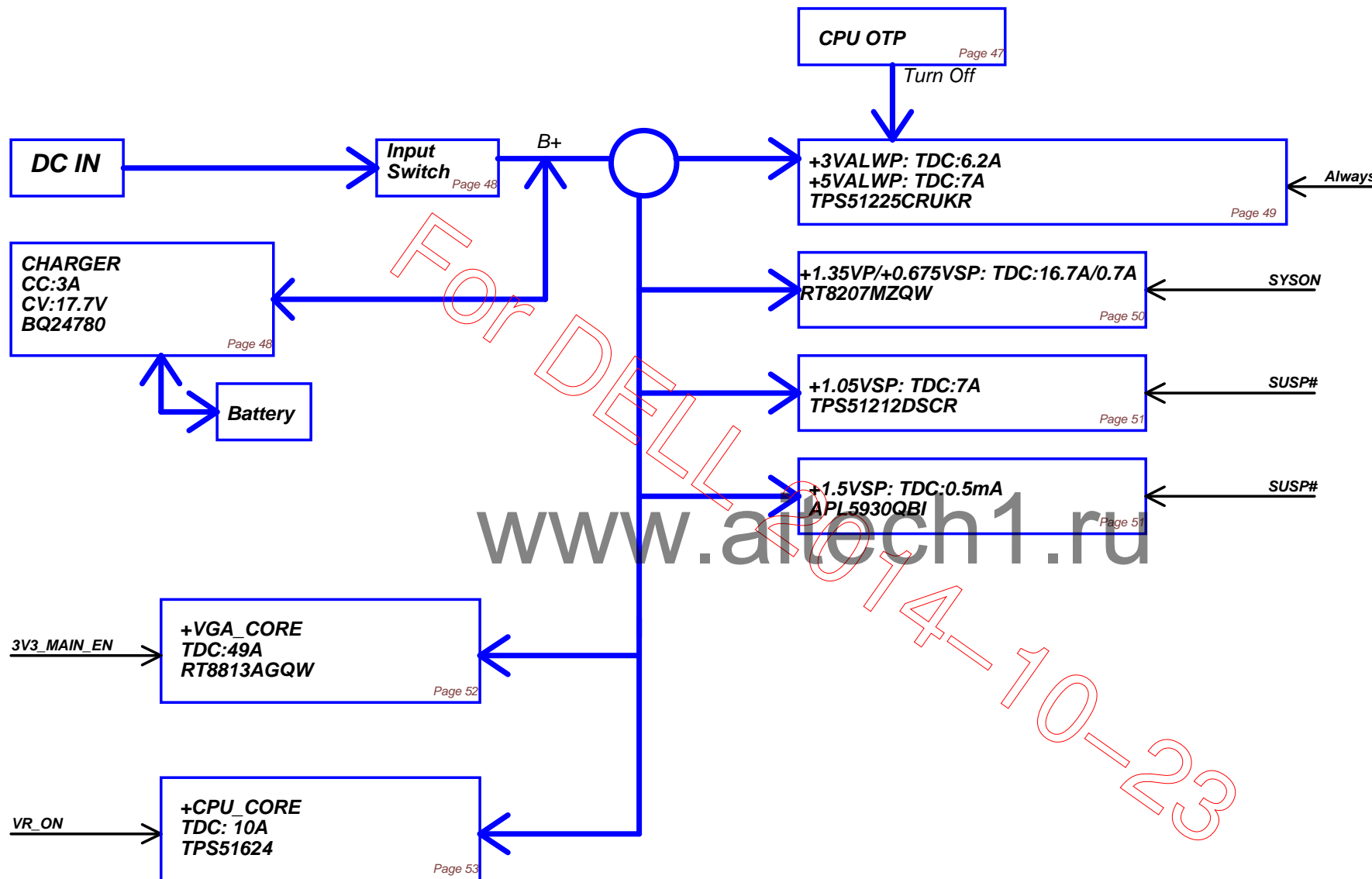
```
CPU_CORE
Frequency = 1.2MHz
OCP Current 39 A
DCR: 0.66m +-7% ohm
PH500 B value: 4250k 1%
PH501 B value: 3435k 1%
```



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# Power block



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